Multibus
BOARD LEVEL COMPUTER PRODUCTS
DATABOOK

NATIONAL SEMICONDUCTOR CORPORATION

National Semiconductor

Introduction

National has been a supplier of MULTIBUS™ products since 1977. Since then our board offerings have expanded to over 100 products—40 of which are included in this booklet.

The MULTIBUS interface offers the user a standard for compatibility which can be maintained throughout a product's evolution. MULTIBUS allows the user to prototype his product and enter the market faster, utilizing the latest technology.

The BLX bus was designed to provide users with low-cost, on-board expansion capabilities. National's BLX boards provide expansion of serial I/O, parallel I/O, peripheral controllers or high-speed math at a fraction of the cost of full-sized boards. The BLX concept keeps system size and cost to a minimum.

National's MULTIBUS board products are all covered under a one year warranty—the longest warranty in the industry. The quality of our board line is driven by corporate commitment to quality. Many customers recognize National as *the* outstanding supplier of top quality products. Such recognition is the result of a management-driven Quality Improvement Program.

The Service Organization provides technical support and repair for Microcomputer Systems Division products. The customer can use our toll-free numbers to contact the response Center for technical assistance with hardware and software design issues or for service. A 48-hour service turn-around is provided on in-warranty products.

Microcomputer Systems Division

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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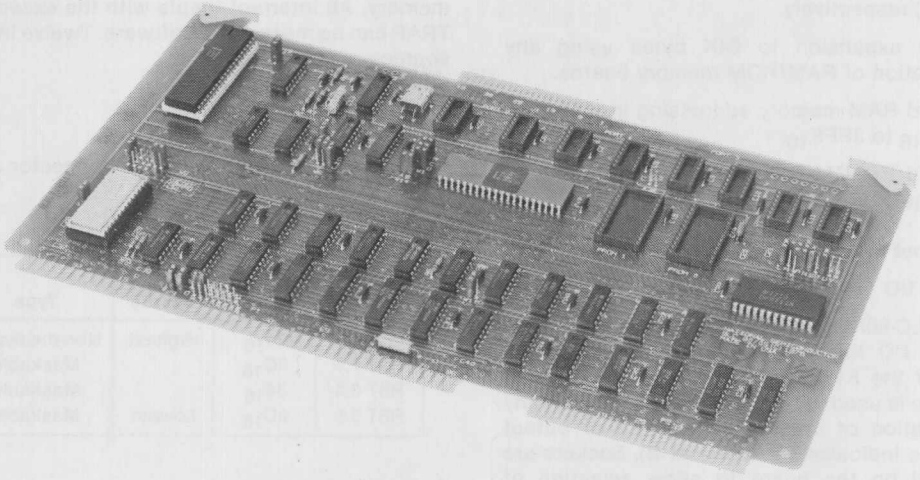
Section 1
Single Board Computers

National Semiconductor

BLC-80/05
Series/80 Board Level Computer



- **Complete System Capability, Including:**
  - 4 vectored interrupts
  - Multiple processor capability — up to six bus masters
  - 14-bit programmable timer
  - 512 bytes of static RAM — up to 8K bytes of EPROM/ROM
  - 22 programmable parallel I/O lines
  - TTL serial I/O interface
- **8085 CPU**
- **Single 5V Power Supply**
- **Compatible With Industry Standard BLC/SBC Series/80 Software and Hardware**
- **Plug-for-Plug Compatible With the Intel SBC-80/05**

Product Overview

The BLC-80/05 is a self-contained board level computer based on the 8085A CPU. Features on the BLC-80/05 allow building powerful and complex systems, particularly those requiring multi-processor configurations. This is provided by special bus arbitration logic incorporated on the board to sort out all contention disputes among processors sharing the same system bus.

Advanced features such as vectored interrupts and an on-board programmable timer greatly reduce the software generation effort for many applications. When combined with the computing power of the 8085A and the I/O capability of the 8085 chip set, the BLC-80/05 becomes an excellent candidate for a high performance, low cost, processor in a multi-processor system.

The BLC-80/05 is compatible with the large family of Series/80 products. This brings into feasibility the construction of systems with virtually limitless applications.

Functional Description

Central Processor

The powerful 8-bit 8085A is the central processor for the BLC-80/05. It is directly software compatible with the popular 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds.

Memory

- 512 bytes are provided by the 8155 RAM/IO/TIMER and two MM2111As.
- Sockets on-board for 2K, 4K, or 8K bytes of EPROM/ROM using MM2708, MM2716, and 2732 (or 2532) respectively.
- Memory expansion to 64K bytes using any combination of RAM/ROM memory boards.
- On-board RAM memory addressing in the range of $3E00_{16}$ to $3FFF_{16}$.
- On-board EPROM/ROM memory addressing in the range of 0000_{16} to $1FFF_{16}$.

Input/Output

- Parallel I/O

  The BLC-80/05 contains 22 programmable parallel I/O lines implemented using the I/O ports of the 8155 RAM/IO/TIMER. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports (as indicated in Appendix B). Sockets are provided on the board to allow selection of drivers and terminators appropriate for each application. All I/O lines are interfaced using a 50 contact edge connector.

- Serial I/O

  The BLC-80/05 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the 8085 CPU. These functions are controlled exclusively by software through execution of the 8085 RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Serial I/O signals are TTL compatible, and sockets are provided on the board for optional connection of RS232C line drivers and receivers.

Interval Timer

The BLC-80/05 provides a fully programmable binary 14-bit interval timer utilizing the 8155 RAM/IO/TIMER. Four functions are availble:

- Programmable one-shot
- Square wave rate generator
- Interrupt on termination of a specified count
- Rate generator

Interrupt System

The BLC-80/05 utilizes the powerful interrupt processing capability of the 8085A CPU. Interrupt requests are routed via a jumper matrix to the four interrupt inputs of the 8085A (TRAP, RST 7.5, RST 6.5, RST 5.5 in order of descending priority). Each input generates a unique memory address (see Table 1). A single 8085 jump instruction at each of these addresses then provides linkage to each interrupt service routing located anywhere in memory. All interrupt inputs with the exception of TRAP can be masked via software. Twelve interrupt sources are provided:

8 — system bus
2 — 8155 I/O ports
1 — 8155 timer
1 — external (available at connector J1)

Table 1

Interrupt Input	Memory Address	Priority	Type
TRAP	24_{16}	Highest	Non-maskable
RST 7.5	$3C_{16}$		Maskable
RST 6.5	34_{16}		Maskable
RST 5.5	$2C_{16}$	Lowest	Maskable

System Bus Arbitration

The Series/80 system allows multiprocessing. Each bus master attached to the bus provides multi-master bus arbitration logic to prevent contention errors. When used in combination, arbitration logic elements on each of the bus masters are interconnected to form a dynamic master/slave relationship.

This logic can be connected in a straight-line priority scheme where bus control is granted in daisy-chaining fashion from the highest to the lowest priority. Any bus master taking control of the bus thereby denies it to the lower priority bus masters in the chain. Using the straight-line priority scheme, there may be up to six masters on a single bus. By using off-board logic, as many as sixteen bus masters are possible. Control of the bus can be gained on a need basis, or permanently via a hardware or software override feature.

BLC-8908 System Monitor Firmware

The BLC-8908 system monitor is availble in a pre-programmed MM2716 PROM. This comprehensive monitor includes facilities to load, execute and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Routines are included to load or save programs using paper tape. It permits the insertion of break points to facilitate debugging. Programs may be executed starting at any location, or single-stepped. A baud rate search capability is built in which automatically determines the baud rate of the terminal being used at initialization.

The commands supported by the BLC-8908 System Monitor are:

- D — Display memory in hex
- G — Execute program (optionally specify new starting address or breakpoint locations)
- I — Insert into memory
- M — Move memory
- N — Single step
- R — Read hex tape
- S — Examine memory and modify if desired
- W — Punch hex tape
- X — Examine CPU registers and modify if desired

BLC-8959 Serial Cable/Connector Kit

A five-foot RS232C cable and a user-installed connector are available to implement a serial interface.

Specifications

Microprocessor

CPU — 8085A (for instruction set, see Appendix A)

Data Word — 8 bits

Instruction —
Word — 8, 16, and 24 bits

Cycle Time — 2.03 microseconds (minimum instruction time)

System Clock — 1.996 MHz ± 0.1%

Registers — 6 general purpose, 8-bit accumulator, 8-bit program counter, 16-bit stack pointer

Number of Instructions — 113

Address Capability — 64K bytes

Memory

RAM — 512 bytes on-board

ROM — Sockets for 8K bytes on-board (ROM/EPROM)

Expansion — Memory boards in any mix of RAM and ROM up to a 64K byte maximum

Access Time — 500 nanoseconds

Input/Output

Interrupts — 4 level hardware vectored interrupts, 3 maskable

Parallel — 22 programmable I/O lines
Latched, unlatched, strobed modes
3- and 8-bit parallel configuration
Optional line drivers and terminators
TTL compatible

Compatible I/O Driver Modules
(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

TYPE	OUTPUT	CURRENT (MA)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Compatible I/O Terminator Modules — BLC-901 220/330 ohm divider
BLC-902 1k ohm pull-up

Serial — SID and SOD functions of the 8085 CPU are used for serial I/O. They are software controlled through RIM and SIM instructions. Baud rate is determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements. Ouputs are TTL compatible. Sockets provided for RS232C line drivers and receivers.

Compatible drivers and receivers:

Driver — National DS1488 or TI SN75188

Receiver — National DS1490 or TI SN75189

System Bus — Multiple bus master capability for up to 6 masters, expandable to 16 masters with an external priority network. All address, data, and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

Interval Timer

Clocks — 1 programmable

Size — 14 bits

Interval — 8.14 microseconds to 133.33 milliseconds

Frequency Variation — 7.50 Hz to 61.44 KHz

Connectors

System Bus — 86 contact double-sided card edge connector on 0.156 inch centers

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers. Recommended mating connector:

3M 3415-0001
AMP 2-86792-3

Serial I/O — 7 pin right-angle connector on 0.156 inch centers (male and female required)

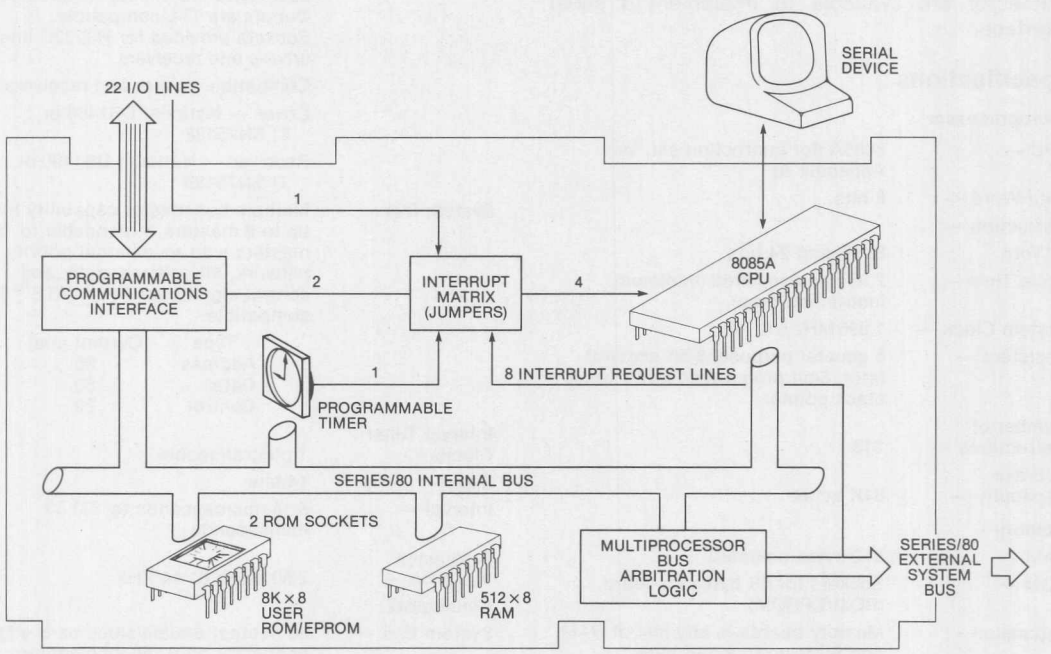
Recommended connector:

MOLEX	09-65-1071	(male)	09-50-7071	(female)
	08-50-0106	(pin)	15-04-0219	(key)
AMP	87194-6	(male)	3-87025-4	(female)
	87023-1	(pin)	87116-2	(key)

Power	+5V ± 5%, 2.65 A +12V ± 5%, 7 mA −12V ± 5%, 23 mA (includes 2 MM2716 EPROMs and BLC-901 terminators installed for 22 input ports with inputs low; ± 12V required only for RS232C capability)		
Environmental Temperature —	0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12.0 oz.	(339.8 gm)

Order Information

BLC-80/05 Series/80 Micro-computer	Includes CPU, 512 bytes of static RAM, sockets for 8K bytes of EPROM, 22 parallel I/O lines, and a serial I/O port
Documentation	
420305817-001	BLC-80/05 Board Level Computer Hardware Reference Manual



BLC-80/05 DIAGRAM

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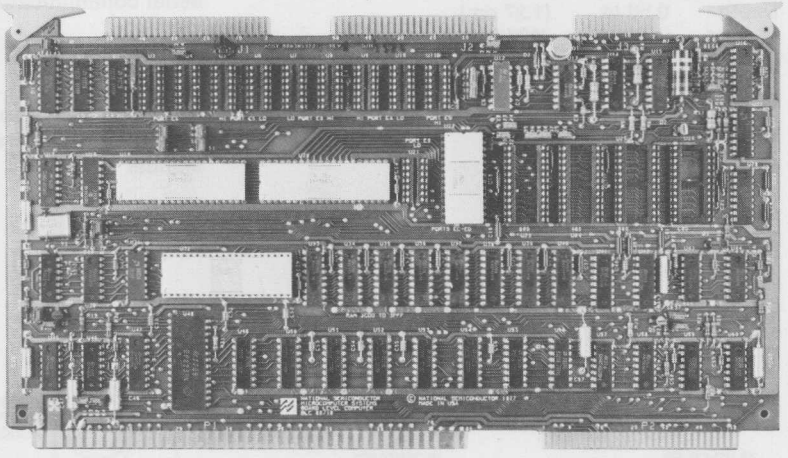
BLC-80/10
Series/80 Board Level Computer



- **Low Cost Computing Power**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 6 interrupt sources
  - 1K static RAM
  - 4K ROM/PROM
- **48 Programmable Parallel I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **Plug-replacement for Intel SBC-80/10**

Product Overview

The BLC-80/10 is a self contained Board Level Computer based on the INS8080A LSI microprocessor. The BLC-80/10 is functionally and physically compatible with the entire family of BLC/SBC hardware and software products.

The BLC-80/10 is a complete computer including a CPU, a serial communications interface, 48 parallel I/O lines, 1K bytes of static Random Access Memory (RAM), sockets to accept 4K bytes of Read Only Memory (ROM/PROM) and a system clock. The BLC-80/10 may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

Functional Description

Central Processor

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/10. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

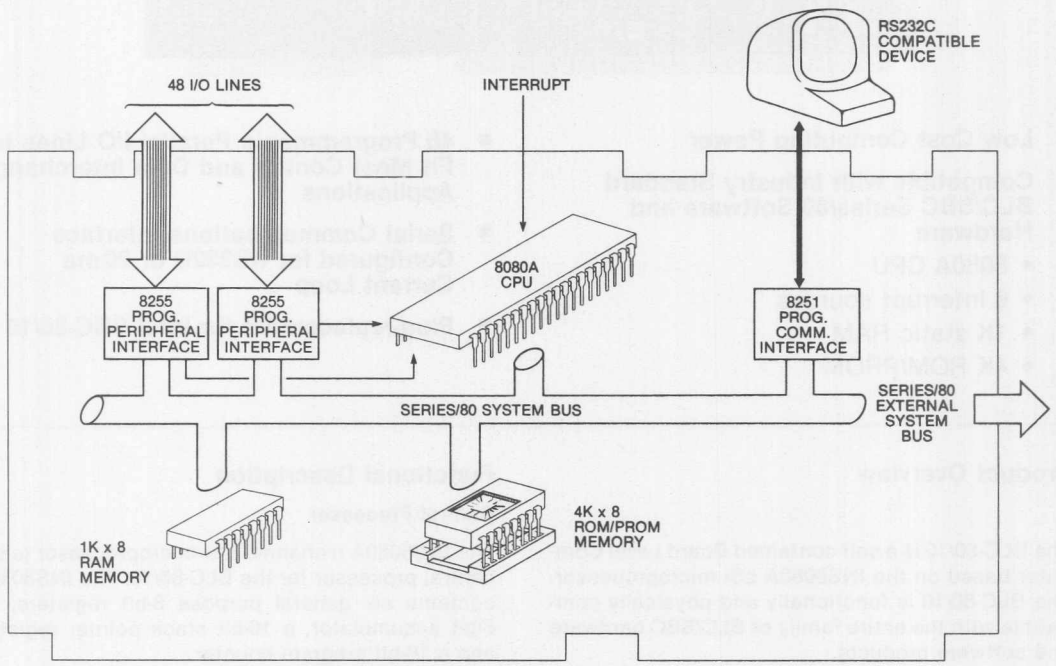
Environmental	Temperature 0° to 55°C		
	Humidity 0 to 90% non-condensing		
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

Order Information

BLC-80/10	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K bytes of ROM, 48 parallel I/O lines and a serial communications interface.

Documentation

420305373-001	BLC-80/10 Board Level Computer Hardware Reference Manual



BLC-80/10 Diagram

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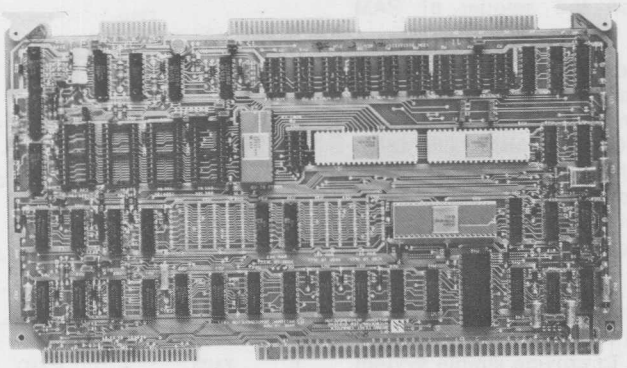
BLC-80/11, BLC-80/14 Series/80 Board Level Computer



- **Low Cost Computing Power with Expanded On-Board Memory**
- **Compatible with Industry Standard BLC/SBC Series/80 Software and Hardware**
  - 8080A CPU
  - 6 interrupt sources
  - 1K, 4K static RAM
  - UP TO 8K ROM/PROM
- **48 Programmable I/O Lines to Fit Most Control and Data Interchange Applications**
- **Serial Communications Interface Configured for RS232C or 20 ma Current Loop**
- **RS232C Interface Selectable for Data Set or Data Terminal**
- **Plug-replacement for Intel SBC-80/10A**

Product Overview

The BLC-80/11 and 80/14 are self contained Board Level Computers based on the INS8080A LSI microprocessor. These computers are functionally and physically compatible with the entire family of BLC/SBC hardware and software products.

The BLC-80/11 and 80/14 are complete computers including a CPU, a serial communications interface, 48 parallel I/O lines, up to 4K bytes of static Random Access Memory (RAM), sockets to accept up to 8K bytes of Read Only Memory (ROM/PROM) and a system clock. These computers may be expanded beyond the basic system through the addition of other products in the BLC/SBC family such as a four or eight slot chassis, power supplies, RAM and ROM expansion in any combination up to 64K bytes, various I/O controllers, digital and analog I/O, and other system modules.

The primary advantage of the BLC-80/11 and 80/14 over the BLC-80/10 is their increased RAM and ROM capacity.

Functional Description

Central Processor

The INS8080A n-channel LSI microprocessor is the central processor for the BLC-80/11 and 80/14. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64K bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/11 and 80/14 contain 1K or 4K bytes, respectively, of on-board static RAM implemented with MM2114 memory modules. On-board memory addressing is predefined in the range 3000_{16} to $3FFF_{16}$, depending upon the amount of RAM installed.

Four sockets are installed to allow user implementation of read only memory for the specific application. Jumpers are provided to allow the use of MM2308/MM2316E ROM's or MM2708/MM2716 EPROM's, giving a maximum of 8K bytes of read only memory in 1K increments. Addressing of the ROM/PROM's is predefined within the range 0000 to $0FFF_{16}$ or $1FFF_{16}$, depending upon the type of ROM installed.

Memory expansion is possible using any mix of standard RAM and ROM expansion boards up to a maximum of 64K bytes. To provide simple system integration, all memory expansion boards can be jumper selected for addressing in the range 0000 through $FFFF_{16}$.

Input/Output

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PPI) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has permanently installed 8226 type drivers. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

	8255 No. 1				8255 No. 2			
Port	1	2	3	Control	4	5	6	Control
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation.

Figure 1. I/O Addresses

National's BLC-901 and BLC-902 terminator modules as well as a number of TTL devices are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines while the BLC-902 contains 1K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table 1 lists the compatible driver modules.

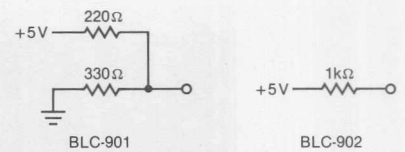


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS232C standards or 20 ma current loop, and interfaces via a 26-contact edge connector. Table 2 lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2 KHz	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

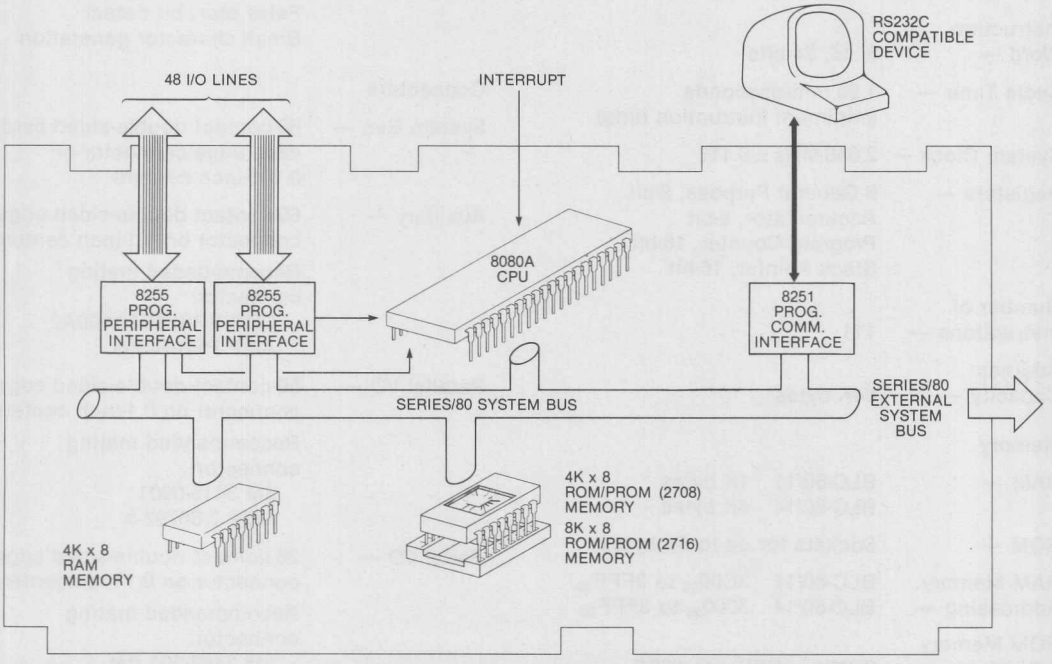
Power	+5V, 2.9A −5V, 0.002A +12V, 0.14A −12V, 0.18A (excluding power required for I/O drivers and user supplied PROM's)		
Environmental	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

Order Information

BLC-80/11	Series/80 Microcomputer Includes CPU, 1K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines and a serial communications interface.
BLC-80/14	Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 4K or 8K bytes of ROM, 48 parallel I/O lines, and serial communications interface.

Documentation

420305532-001	BLC-80/11, 80/14 Board Level Computer Hardware Reference Manual



BLC-80/14 Diagram

Interrupt System

The BLC-80/11 and 80/14 can handle 6 interrupt requests on a single interrupt level. Two are available for external user devices, one through the parallel I/O connector and one on the system bus. The remaining 4 interrupt sources are generated from on-board devices and are jumper selected. The on-board sources are as follows:

- 2 from the INS8255 PPI devices signifying input buffer full or output buffer empty
- 2 from the INS8251 USART device signifying input data ready or output character needed

The 6 interrupt sources share a common CPU level which causes a RESTART 7 instruction to be executed. The user response to the interrupt is handled by an interrupt processing routine starting at memory location 0038_{16}.

Specifications

Microprocessor

CPU —	INS8080A (for Instruction Set see Appendix A)
Data Word —	8 bits
Instruction Word —	8, 16, 24 bits
Cycle Time —	1.95 microseconds (minimum instruction time)
System Clock —	2.048 MHz ± 0.1%
Registers —	6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit
Number of Instructions —	111
Address Capacity —	64K bytes

Memory

RAM —	BLC-80/11 BLC-80/14	1K bytes 4K bytes
ROM —	Sockets for up to 8K bytes	
RAM Memory Addressing —	BLC-80/11 BLC-80/14	$3C00_{16}$ to $3FFF_{16}$ 3000_{16} to $3FFF_{16}$
ROM Memory Addressing —	0000 to $0FFF_{16}$ or $1FFF_{16}$	
Expansion —	Memory boards in any mix of RAM and ROM up to 64K bytes maximum	
Access Time —	500 nanoseconds (maximum)	

Input/Output

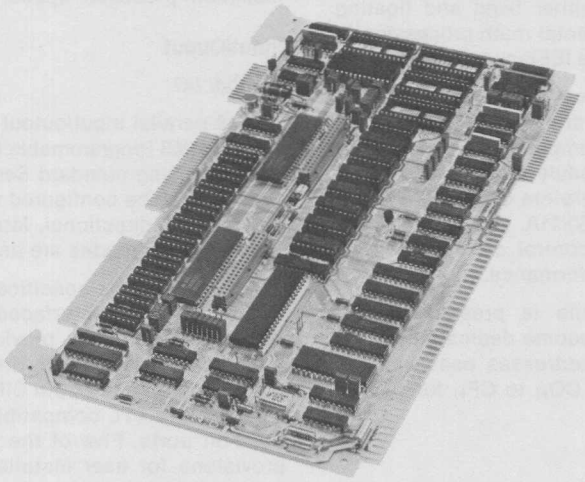
Interrupts —	Single level, 6 sources Programmable masking Active low TTL levels
Parallel —	48 lines Latched, unlatched, strobed modes 4- and 8-bit parallel configuration Optional line drivers and terminators TTL compatible
Serial —	20 ma current loop or RS232C
Synchronous Mode	5-8-bit character Internal/external synchronization Automatic SYNC insertion SYNC search
Asynchronous Mode	5-8-bit character 1, 1½, or 2 stop bits False start bit detect Break character generation

Connectors

System Bus —	86-contact double-sided card cage edge connector on 0.156-inch centers
Auxiliary —	60-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: CDC VPB01B30A00A2 AMP PES-14559
Parallel I/O —	50-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3
Serial I/O —	26-contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-001 flat AMP 2-86792-3 round

National Semiconductor

BLC-80/11A, BLC-80/14A Series/80 Board Level Computers



- **Upward compatible with BLC-80/11 board level computer**
- **Two BLX bus connectors for on-board expansion with BLX series modules**
- **1 K and 4 K bytes of RAM**
- **Sockets for up to 32 K bytes of PROM**
- **48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators**
- **Programmable synchronous/ asynchronous communications port with selectable RS-232C or 20 mA current loop interface**
- **Single level interrupt with 16 interrupt sources**
- **Auxiliary power bus and power-fail interrupt control logic for RAM battery backup**
- **Limited master Multibus™ interface**
- **Compatible with industry standard BLC/SBC Series/80 hardware and software**
- **Plug replacement for SBC-80/10B**

Product Overview

The BLC-80/11A Family of Board Level Computers (BLC-80/11A, BLC-80/14A) are members of a family of Series/80 products with the BLX interface. This interface (identical to the SBX standard) provides the means for economical expansion of on-board resources. The OEM can combine the BLC-80/11A with any of the BLX series of expansion modules and customize his application with off-the-shelf products from National Semiconductor Corporation.

The BLC-80/11A Family is essentially the BLC-80/11 Family (BLC-80/11, BLC-80/14) with several enhancements. These, in general, include two BLX connectors, support for 2764 PROMs, and battery backup logic.

Multibus is a trademark of Intel Corp.

Functional Description

BLX Module Expansion Bus

The new BLX bus interface brings an entirely new dimension to system design, offering incremental, on-board expansion with small BLX modules. Two BLX bus connectors are provided to allow plug-in expansion with any BLX module. One may use these to expand existing on-board resources, or configure entirely new functions.

Examples of expanding existing BLC-80/11A resources would be adding the BLX-350 Parallel I/O Module, or the BLX-351 Serial I/O Module. These provide respectively 24 additional programmable parallel I/O lines, with sockets for user customization of

the interface, and an additional synchronous/asynchronous serial port, either RS-232C or RS-449/442.

A means of adding new functionality would be to install the BLX-331 or BLX-332 Math Processor Modules. These provide either fixed and floating point math with transcendental math processing or floating point math with the IEEE-suggested format.

The BLX module is a logical extension of the on-board programmable I/O, and is accessed by the BLC-80/11A Board Level Computer as a common I/O port location. The BLX module is coupled directly to the 8080A CPU, and therefore becomes an integral element of the BLC-80/11A. This negates the need for contending for control of the Multibus, providing for optimum performance.

Only when a BLX module is present do the assigned I/O addresses become dedicated to that BLX connector. The I/O addresses used when a module(s) is installed are CO_H to CF_H for J4 and FO_H to FF_H for J5.

Central Processor

The INS8080A N-channel LSI microprocessor is the central processor for the BLC-80/11A. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64 K-bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64 K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/11A, and BLC-80/14A are shipped with 1 K-byte and 4 K-bytes, respectively, of static RAM. RAM starting address is jumper-selectable to begin immediately after PROM, regardless of the amount of PROM installed, or on any boundary defined by the amount of RAM installed. All on-board RAM read and write operations are performed at maximum processor speed.

Four 28-pin sockets are provided to allow user installation of read only memory for specific applications. Allowable device types are 1 K × 8 (2708, 2758), 2 K × 8 (2716), 4 K × 8 (2732), and 8 K × 8 (2764), or pin compatible ROMs. This provides on-board installation of as much as 32 K-bytes of permanent storage. If less than four devices are present, jumpers allow dedication of the unused space to other resources. All on-board ROM, or EPROM, read operations are performed at maximum processor speed.

Input/Ouput

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PP) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has a permanently installed 8303 type driver. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

Figure 1. I/O Addresses

	8255 No. 1				8255 No. 2			
Port	**1**	**2**	**3**	**Control**	**4**	**5**	**6**	**Control**
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation

National's BLC-901 and BLC-902 terminator modules, as well as a number of TTL devices, are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines, while the BLC-902 contains 1 K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table I lists the compatible driver modules.

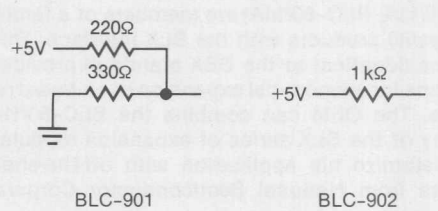


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (mA)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/ Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS-232C standards or 20 mA current loop, and interfaces via a 26-contact edge connector. The data interface is located at I/O address EC_H, control at ED_H. Table II lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable) (KHz)	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

Interrupt requests may originate from 16 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Three jumper selectable interrupt requests can automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), a character is ready to be transmitted (i.e. the USART is ready to accept a character from the CPU), or when the transmitter is empty (i.e., the USART has no character to transmit). These five interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the Multibus system bus and the other via the I/O edge connector. One jumper selectable interrupt request may be interfaced to the power-fail interrupt control logic. Two general purpose and two optional interrupt requests are jumper selectable from each of the BLX interfaces. These eight signals permit user installed expansion modules to interrupt the 8080A CPU. The sixteen interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a restart instruction (RESTART 7) is generated. The processor responds by suspending program execution and executing user defined interrupt service routine originating at location 38_H.

Power-Fail Circuitry

A power-fail interrupt may be detected through the AC-low signal generated by the power supply. This signal may be configured to interrupt the 8080A CPU to initiate an orderly power down instruction sequence. Additionally, if battery backup power is being supplied through the auxiliary connector (P2), read and write operations to RAM are disabled, and RAM contents are maintained.

Specifications

Microprocessor

CPU — INS8080A

Data Word — 8 bits

Instruction Word — 8, 16, 24 bits

Cycle Time — 1.95 microseconds (minimum instruction time)

System Clock — 2.048 MHz ± 0.1%

Registers — 6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit

Number of Instructions — 111

Address Capacity — 64 K bytes

Memory

RAM — BLC-80/11A — 1 K bytes
BLC-80/14A — 4 K bytes

ROM/PROM — Sockets for up to 32 K bytes

RAM Memory Addressing — Any boundary within $FFFF_H$ where boundary defined by amount of RAM installed (i.e. if 2 K bytes installed, locate on any 2 K byte boundary)

ROM Memory Addressing — 0_H-$0FFF_H$ using 2708, 2758
0_H-$1FFF_H$ using 2716
0_H-$3FFF_H$ using 2732
0_H-$7FFF_H$ using 2764
(Assuming all sockets used)

Off-Board Expansion — Memory boards in any mix of RAM and ROM/PROM up to a system total of 64 K bytes

Input/Output

Interrupts — Single level, 16 sources
- 2 — User specified I/O
- 2 — Parallel I/O
- 3 — Serial I/O
- 1 — Power-fail interrupt
- 8 — BLX connectors (2)

Parallel — 48 lines
Latched, unlatched, strobed modes
4- and 8-bit parallel configuration
Optional line drivers and terminators
TTL compatible

Serial — 20 mA current loop or RS-232C

Synchronous Mode — 5-8-bit character
Internal/external synchronization
Automatic SYNC insertion
SYNC search

Asynchronous Mode — 5-8-bit character
1, 1½, or 2 stop bits
False start bit detect
Break character generation

BLX Expansion — 2 BLX expansion connectors. Accepts 2 single-size or 1 double size BLX module.

I/O Addressing — (On-board programmable I/O)

Device	I/O Address
8255 No. 1	
Port A	E4
Port B	E5
Port C	E6
Control	E7
8255 No. 2	
Port A	E8
Port B	E9
Port C	EA
Control	EB
8251	
Data	EC
Control	ED
BLX Connector J4	
MCS0	C0-C7
MCS1	C8-CF
BLX Connector J5	
MCS0	F0-F7
MCS1	F8-FF

Connectors

System Bus — 86-contact double-sided card cage edge connector on 0.156-inch centers

Auxiliary — 60-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559

Parallel I/O — 50-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

Serial I/O — 26-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3462-001 flat
AMP 2-86792-3 round

Power —

VDC	Normal	Battery
+5V ± 5%	3.46 A	25 mA + 140 mA/ KB RAM
−5V ± 5%	2 mA	—
+12V ± 5%	150 mA	—
−12V ± 5%	175 mA	—

Note 1: Based on the following installed: four 2758, 2716, or 2732 EPROMs, 1 KB of RAM, BLC-901 on 48 input lines (inputs low)

Environmental Temperature — 0° to 55°C
Humidity — 0% to 90%, non-condensing

Physical Height: 6.75 in. (17.15 cm)
Width: 12.00 in. (30.48 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (396.9 g)

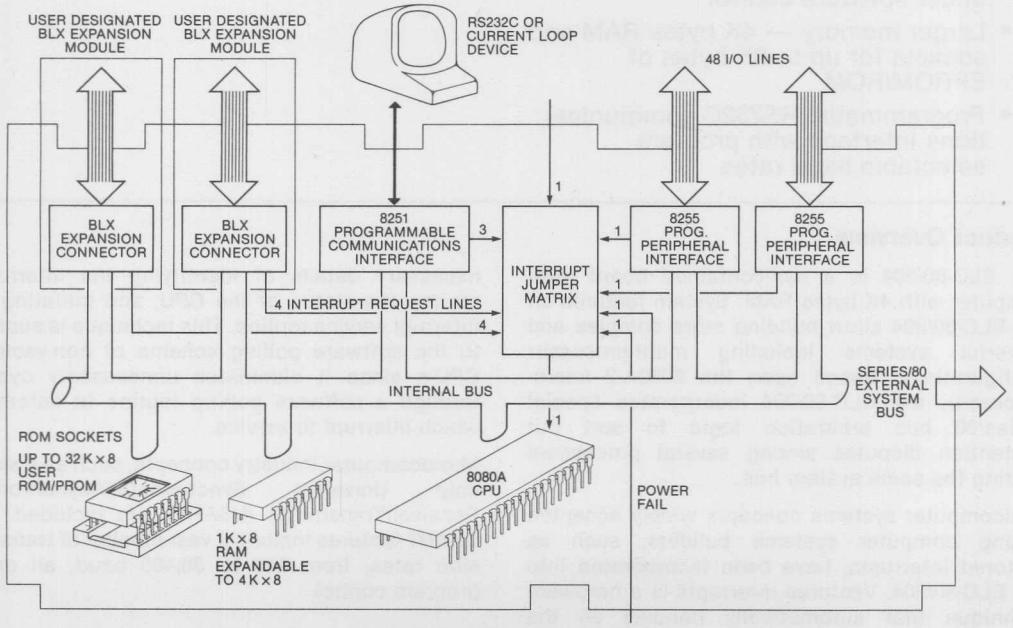
Order Information

BLC-80/11A — Series/80 Board Level Computer Includes CPU, 1 K bytes of static RAM, sockets for up to 32 K bytes of ROM, 48 parallel I/O lines, one serial port and 2 BLX expansion connectors.

BLC-80/14A — Series/80 Board Level Computer Includes CPU, 4 K bytes of static RAM, sockets for up to 32 K bytes of ROM, 48 parallel I/O lines, one serial port, and 2 BLX expansion connectors.

Documentation

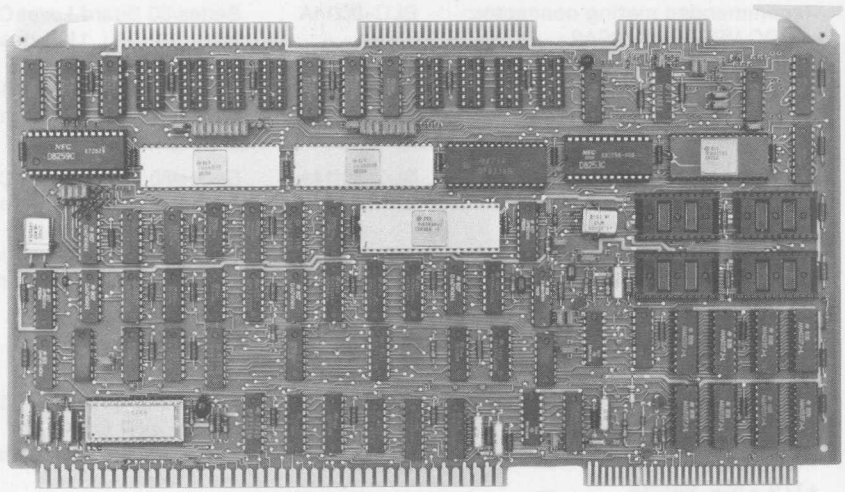
420306321-001 — BLC-80/11A, BLC-80/14A Board Level Computer Hardware Reference Manual



BLC-80/11A Block Diagram

National Semiconductor

BLC-80/204
Series/80 Board Level Computer



- **Complete System Capability, including:**
  - 8 vectored interrupts
  - Multiple processor capability — up to six bus masters
  - Interval timer with three programmable counters
  - ROM/RAM "shadowing" capability under software control
  - Larger memory — 4K bytes RAM and sockets for up to 8K bytes of EPROM/ROM
  - Programmable RS232C communications interface with program selectable baud rates
- **Low Power MM5257 Static RAM with Battery Backup Circuitry**
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**
- **Plug-for-Plug Compatible with the Intel SBC-80/20 and SBC-80/204**

Product Overview

The BLC-80/204 is a self-contained board level computer with 4K bytes RAM. System features on the BLC-80/204 allow building more complex and powerful systems including multi-processor configurations. Based upon the 8080A-2 microprocessor, the BLC-80/204 incorporates special Series/80 bus arbitration logic to sort out contention disputes among several processors sharing the same system bus.

Minicomputer systems concepts widely accepted among computer systems builders, such as vectored interrupts, have been incorporated into the BLC-80/204. Vectored interrupts is a hardware technique that automatically handles all the necessary details of identifying the interrupts, storing the status of the CPU, and initiating the interrupt service routine. This technique is superior to the software polling scheme of non-vectored CPU's since it eliminates unnecessary cycling through a software polling routine to determine which interrupt to service.

Microcomputer industry concepts, such as a single chip Universal Synchronous/Asynchronous Receiver/Transmitter (USART), are included. The USART features include a vast number of transmission rates, from 110 to 38,400 baud, all under program control.

The BLC-80/204 is a complete computer including:

- CPU
- Serial I/O
- Parallel I/O
- Interval timers
- Vectored interrupts
- RAM and ROM memory

The basic BLC-80/204 microcomputer can be expanded by the addition of a four slot chassis, power supply, ROM and RAM memory, various I/O controllers, analog and digital I/O and other system modules — even more BLC-80/204's. Thus, the basic advantage of the BLC-80/204 is that it provides low cost single board computer capability, yet is expandable to a substantially more powerful multiprocessor configuration.

Functional Description

Central Processor

- CPU: 8080A-2 Microprocessor
- Maximum addressing range — 64K bytes
- Data word — 8 bits
- Instruction word — 8, 16, 24 bits
- Addressing modes — direct, register, register indirect and immediate
- Instruction types — total of 111 instructions
  - — 18 data transfer
  - — 29 arithmetic
  - — 19 logical
  - — 29 branch
  - — 16 central
- Registers
  - — 7 general registers — 1 accumulator (A) plus six 8-bit work registers which may be utilized individually (B, C, D, E, H, L) or in pairs (B and C, D and E, H and L), effectively forming three 16-bit registers.
  - — 1 16-bit program counter.
  - — 1 16-bit stack pointer.
- Subroutine mechanism
  - — Hardware stack pointer with push and pop instruction
  - — Call and return instructions

Memory

- 4K bytes of static read/write memory using MM5257 RAM with auxiliary battery backup power bus (560 ma, 1.5 V)
- Sockets on-board for up to 8K bytes of ROM in 1K or 2K increments using MM2708 or MM2716 EPROM
- Memory expansion to 64K bytes using any combination of RAM/ROM memory boards
- A memory shadow technique is incorporated allowing on-board ROM memory addresses to be identical to off-board ROM/RAM memory addresses. By switching back and forth via software, a ROM bootstrap routine can "disappear" from memory to be replaced with RAM once the system start-up procedure is past the bootstrap stage.
- On-board RAM memory addressing in the range 2000_{16} through $FFFF_{16}$ selectable on 4K byte boundaries. Off-board RAM memory addressing from 0000 to $FFFF_{16}$.
- ROM/PROM memory addressing in the range 0000 through $1FFF_{16}$.
- An automatic synchronizing signal is generated by the processor during non-memory access time periods to allow the off-board dynamic RAM expansion memory to go through a refresh cycle without reducing system throughput. This unique refresh synchronizing technique effectively allows the dynamic expansion memory to exhibit static memory characteristics.

Input/Output

- Parallel I/O
  - — Two INS8255 programmable peripheral interface circuits provide a total of 48 I/O lines which can be configured by software into any combination of unidirectional/bidirectional I/O ports. Sockets are provided on the board to allow selection of drivers and terminators appropriate for each application. All I/O lines are interfaced using a pair of 50 contact edge connectors for mating with cables. The operating modes are defined in Appendix B.
- Serial I/O
  - — One INS8251 Universal Synchronous/Asynchronous Receiver/Transmitter provides the serial I/O port with programmable communications rates, data formats, control characters and parity. Logic is provided for detection of framing, overrun and parity errors, as well as double buffering. The serial I/O port provides RS232C signals interfaced via a 26 contact edge connector.

Interval Timer (Clocks)

One 8253 programmable interval timer provides three programmable 16-bit counters. One is used as a baud rate generator for the serial I/O port and

the other two are used as general purpose BCD or binary 16-bit counters. The other two can be cascaded into one 32-bit counter. Each clock has up to seven software selectable functions:

- Interrupt on termination of a specified count
- Programmable one-shot
- Rate generator based upon a multiple of the input clock period
- Square wave rate generator
- Software triggered strobe
- Hardware triggered strobe
- Event counter (using external signal to drive clock input)

Input Frequencies —	Reference 1.0752 MHz ± 0.1% Event rate 1.1 MHz maximum
Output Frequencies/ Timing Intervals —	Variable time intervals from 1.86 microseconds to 1.109 hours. Frequency variation from 25 KHz to 537.61 KHz.

Interrupt System

A programmable interrupt module handles interrupt vectoring of eight interrupt levels. Four priority processing modes may be reconfigured under program control during system operation. Interrupts in any combination may be masked under program control.

The programmable interrupt module accepts interrupts from parallel and serial I/O, programmable timers, or the system bus. Each interrupt is serviced based on its priority, which is determined by attaching the device interrupt line to one of eight system bus interrupt lines.

Each of the eight BLC-80/204 levels is connected to a specific line on the system bus. Each level may be connected to as many as 16 interrupts, but the system will not detect more than one interrupt at a time on the same level. A software polling routine may be used to distinguish among multiple interrupts on the same level if more than eight are desired. On-board interrupt sources are available as follows:

4 — two from each of two 8255 parallel I/O modules

2 — two from the 8251 serial I/O module

2 — one from each of two available system clocks

Interrupts may come from up to 8 sources on the Series/80 system bus and up to 48 from the I/O ports on the two 8255's.

A block of memory (32 or 64 bytes) must be reserved for interrupt vectors. The address for each level is spaced at intervals of 4 or 8 bytes (program selectable). A single JUMP instruction at each location links the ultimate service routine.

Table 1. Programmable Interrupt Modes

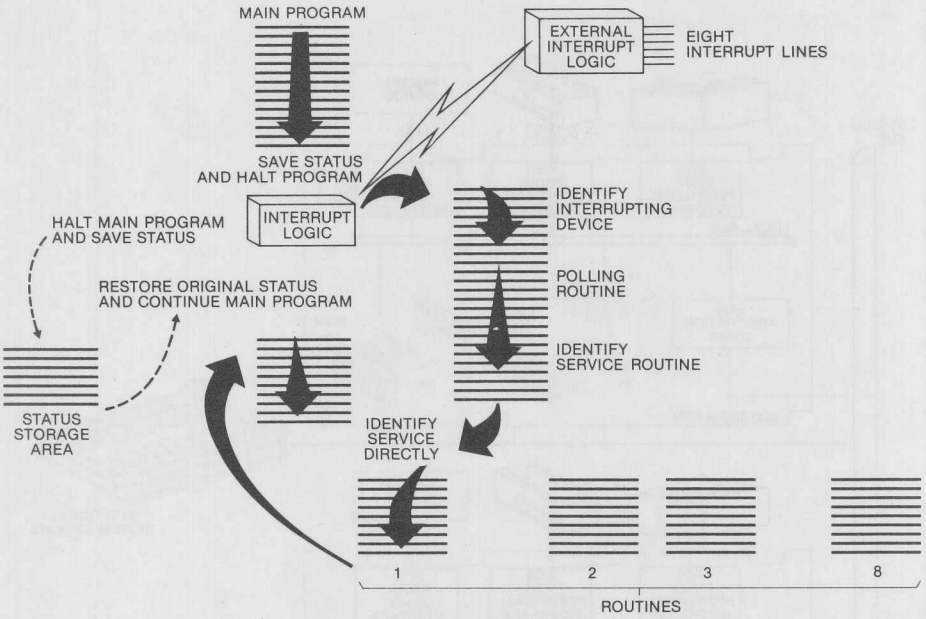
Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 (highest) through 7 (lowest).
Auto-Rotating	Once serviced, a given level becomes the lowest priority level until the next interrupt occurs.
Specific Priority	Software assigns the lowest priority level.
Polled	Software examines an interrupt status by using the interrupt status register.

System Bus Arbitration

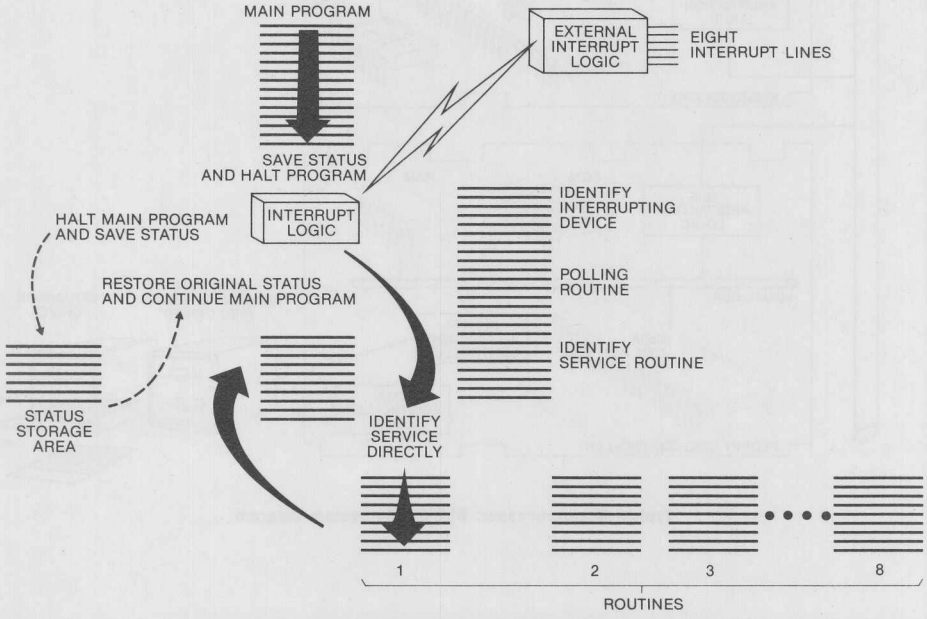
The Series/80 system bus allows multiple devices to transfer data on a common bus.

The Series/80 system bus allows multiprocessing. Each bus master attached to the Series/80 system bus must provide multi-master bus arbitration logic to prevent contention errors. When used in a system configuration, bus arbitration logic elements on each of the bus masters are interconnected to form a dynamic master/slave relationship.

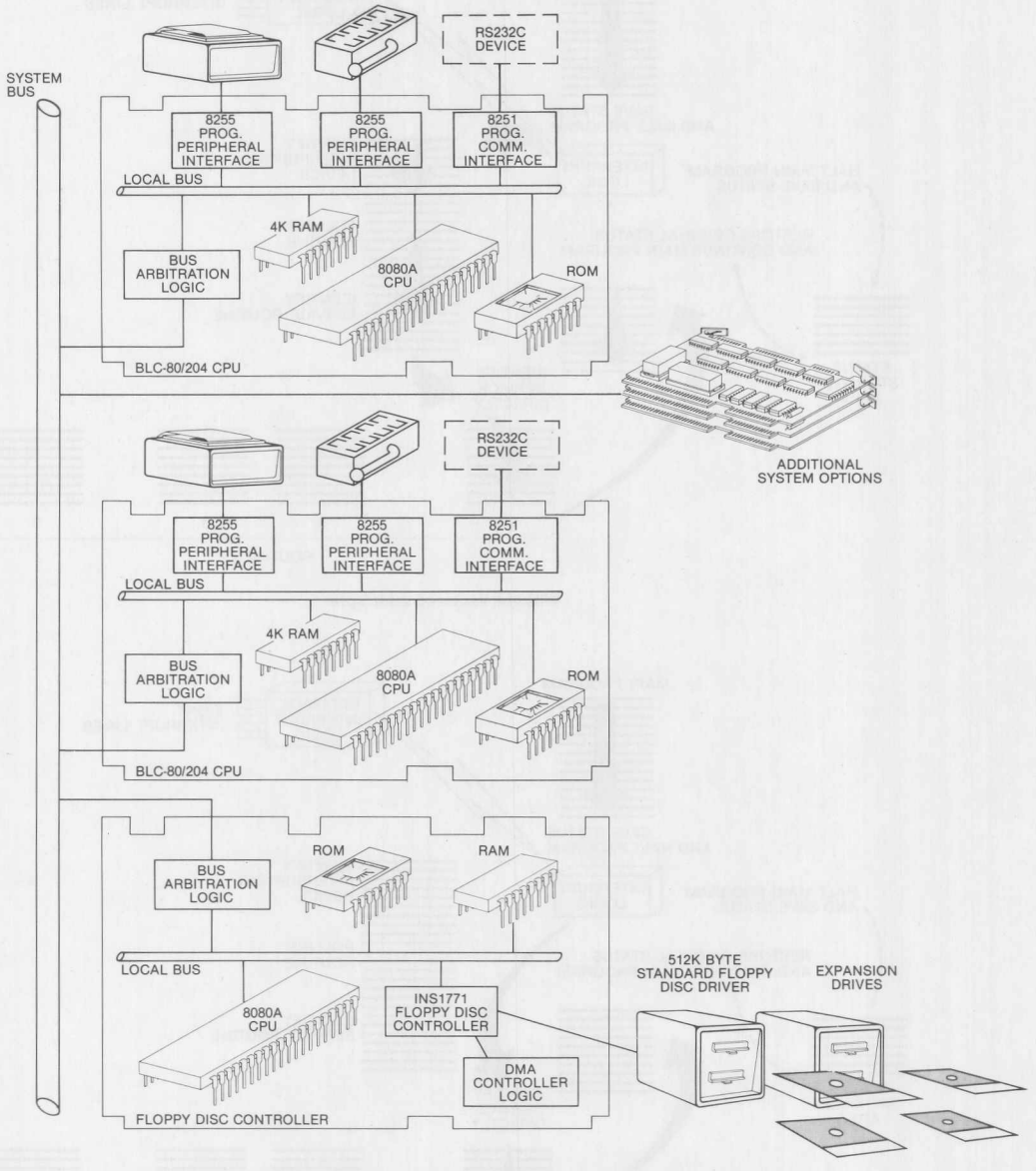
The bus arbitration logic modules can be connected in a straight-line priority scheme where bus control is granted in daisy-chaining fashion from the highest priority to the lowest priority. Any bus master taking control of the bus thereby denies it to bus masters lower in priority in the chain. Using the straight-line priority scheme, there may be up to six bus masters on a single system. By using off-board logic, as many as sixteen bus masters are possible.



Without Vectored Interrupts



Vectored Interrupts



Typical Microprocessor: BLC-80/204 System Diagram

Specifications

Microprocessor

CPU — 8080A-2 (for Instruction Set, see Appendix A)

Data Word — 8 bits

Instruction Word — 8, 16 and 24 bits

Cycle Time — 1.86 microseconds (minimum instruction time)

System Clock — 2.1504 MHz ± 0.1%

Registers — 6 General Purpose, 8-bit
Accumulator, 8-bit
Program Counter, 16-bit
Stack Pointer, 16-bit

Number of Instructions — 111

Address Capacity — 64K bytes

Memory

RAM — 4K bytes on-board

ROM — Sockets for 8K bytes on-board (ROM/PROM/EPROM)

Expansion — Memory boards in any mix of RAM and ROM up to a 64K byte maximum

Access Time — 500 nanoseconds (maximum)

Input/Output

Interrupts — 8 level hardware vectored interrupts
Programmable masking
4 priority modes

Parallel — 48 programmable I/O lines
Latched, unlatched, strobed modes
4- and 8-bit parallel configuration
Optional line drivers and terminators
TTL compatible

Compatible I/O Driver Modules
(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Type	Output	Current (ma)
7438	I, OC, HV	48
7437	I	48
7432	NI	16
7426	I, OC, HV	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Compatible I/O Terminator Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial — Programmable
Full data set control
Double buffered
RS232C compatible
Synchronous mode:
5-8-bit character
Internal/external synchronization
Automatic SYNC insertion
SYNC search
75-9600 baud
Asynchronous mode:
5-8-bit character
1, 1½ or 2 stop bits
False start bit detect
1760-38400 baud
Break character generation

System Bus — Multiple bus master capability for up to 6 masters, expandable to 16 masters with additional priority network. All address, data and control signals are TRI-STATE™ TTL compatible:

Type	Current (ma)
Address	50
Data	50
Control	32

Interval Timer (Clocks)

Clocks — 3 programmable

Size — 16 bits

Interval — 1.86 microseconds to 1.109 hours

Frequency Variation — 25 KHz to 537.61 KHz

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — (Battery back-up) 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559
TI H311130

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

Serial I/O — 26 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power

VDC	Normal	Battery
+5V	4.9A	0.56A
−5V	0.18A	—
+12V	0.35A	—
−12V	0.02A	—

(normal based on 4K ROM installed)

Environmental

Temperature 0° to 55°C
Humidity 0 to 90%, non-condensing

Physical

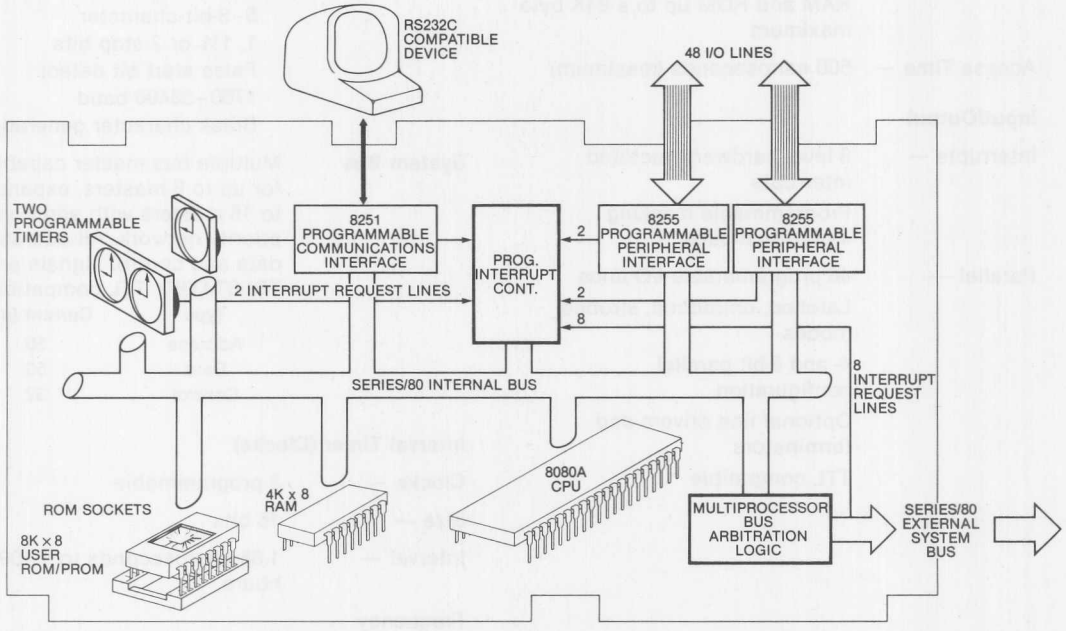
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-80/204 — Series/80 Microcomputer Includes CPU, 4K bytes of static RAM, sockets for 8K bytes of ROM, 48 parallel I/O lines and an RS232C serial I/O

Documentation

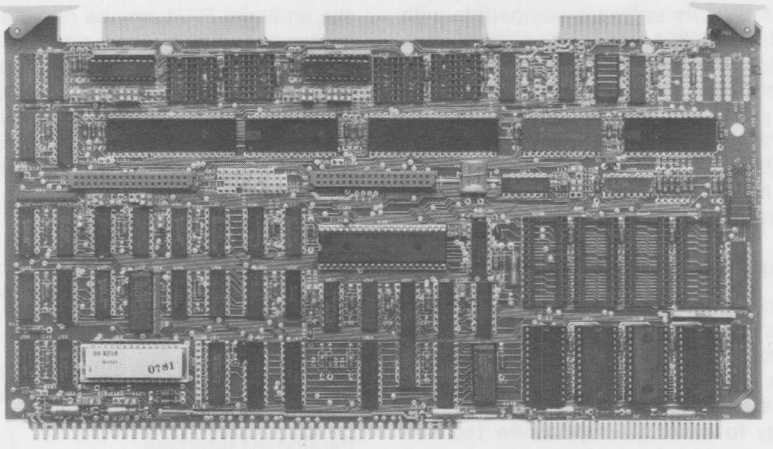
420305521-001 — BLC-80/204 Board Level Computer Hardware Reference Manual



BLC-80/204 Diagram

National Semiconductor

BLC-80/24, BLC-80/28 Board Level Computers



- **Upward compatible with BLC-80/204 Board Level Computer**
- **8085A-2 CPU operating at 4.8 or 2.4 MHz**
- **Two BLX bus connectors for BLX expansion modules**
- **4K bytes of static read/write memory with BLC-80/24, 8K bytes with BLC-80/28**
- **Sockets for up to 32K bytes of read only memory, supports 2758s, 2716s, 2732s, 2764s**
- **RAM/ROM shadowing**
- **48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators**
- **Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rates**
- **Full MULTIBUS™ control logic for multimaster configurations and system expansion**
- **Two programmable 16-bit BCD or binary timers/event counters**
- **12 levels of programmable interrupt control**
- **Auxiliary power bus, memory protect, and power-fail interrupt control logic provided for battery backup RAM requirements**
- **Plug-replacements for Intel SBC-80/24**

Product Overview

The National BLC-80/24 and BLC-80/28 Board Level Computers are members of National's complete line of OEM microcomputer systems which take full advantage of the latest LSI technology to provide economical, self-contained computer-based solutions for test systems, industrial control, and OEM applications. The BLC-80/24 and BLC-80/28 boards are complete computer systems on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, BLX bus interface, read/write memory, read only memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic, and programmable timers all reside on the board. Full MULTIBUS interface logic is included to offer compatibility with the National OEM Microcomputer Systems family of Board Level Computers, expansion memory options, digital and analog I/O expansion boards, and peripheral and communications controllers.

Functional Description

Central Processing Unit

The powerful 8-bit N-channel 8085A-2 CPU fabricated on a single LSI chip, is the central processor for the BLC-80/24 and 80/28 boards. Operating at either 4.8 or 2.4 MHz (jumper selectable), the 8085A-2 CPU is directly software compatible with the 8080A CPU. The 8085A-2 contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing single and double precision operators. Minimum instruction execution time is 826 nanoseconds. A block diagram of the BLC-80/24 and 80/28 functional components is shown in Figure 1.

Board Level Expansion Modules

The new BLX bus interface brings an entirely new dimension to system design offering incremental on-board expansion at minimal cost. Two BLX bus connectors are provided for plug-in expansion of any BLX expansion modules. The BLX concept provides the ability to adapt quickly to new technology, the economy of buying only what is needed, and the ready availability of a spectrum of functions for greater application potential. BLX Modules are available to provide expansion equivalent to the I/O available on the BLC 80/24, 80/28 boards or the user may configure entirely new functionality, such as math, directly on board. The BLX-350 Parallel I/O Expansion Module provides 24 I/O lines using an 8255A Programmable Peripheral Interface. Therefore, two BLX 350 modules together with the BLC 80/24, 80/28 boards may offer 96 lines of programmable I/O. Alternately, a serial port may be added using the BLX-351 Serial I/O Expansion Module and math may be configured on-board with the BLX-332 Floating Point Math or BLX-331 Fixed/Floating Point Math Expansion Module. Future BLX products are also planned. The BLX Expansion Module is a logical extension of the on-board programmable I/O and is accessed by the BLC-80/24, 80/28 as common I/O port locations. The BLX Module is coupled directly to the 8085A-2 CPU and therefore becomes an integral element of the BLC-80/24, 80/28 providing optimum performance.

Memory Addressing

The 8085A-2 has a 16-bit program counter and a bank select option which allows direct addressing of up to 128K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The BLC-80/24 board contains 4K bytes of static RAM and the BLC-80/28 contains 8K bytes of static RAM. All RAM read and write operations are performed at maximum processor speed. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. In addition, the RAM is addressable at the 4K boundaries. A memory shadow technique is also incorporated allowing on-board ROM memory addresses to be identical to off-board ROM/RAM memory addresses.

Four sockets are provided for up to 32K bytes of nonvolatile read only memory on the BLC 80/24 and 80/28 boards. EPROM may be added in 1K byte increments up to 4K (using 2758s); in 2K byte increments up to 8K bytes (using 2716s); in 4K byte increments up to 16K bytes (using 2732s); or in 8K byte increments up to 32K bytes (using 2764s).

Parallel I/O Interface

The BLC-80/24 and 80/28 boards contain 48 programmable parallel I/O lines implemented using two 8255A Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports as indicated in Table 1; therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optimal line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, woven, or round cables.

Serial I/O Interface

A programmable communications interface using an 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the BLC-80/24 and 80/28 boards. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES:

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable. The BLC-530 Current Loop Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The BLC-530 adapter may be used to interface the BLC-80/24 and 80/28 boards to teletypewriters or other 20 mA current loop equipment.

Multimaster Capability

The BLC-80/24 and 80/28 boards are full computers on a single board with resources capable of supporting a large variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e. several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the BLC-80/24 and 80/28 boards provide full MULTIBUS arbitration control logic. This control logic allows up to 6 bus masters to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the MULTIBUS system bus with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the BLC-80/24 and 80/28 boards or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus since transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design protects slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct memory access (DMA) operations, and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The BLC-80/24 and 80/28 boards provide three independent, fully programmable 16-bit interval timers/event counters utilizing an 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller, to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, or may be routed as inputs to the 8255A chip. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the RS232C USART serial port. In utilizing a

BLC-80/24 or 80/28 board, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for even counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Even counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Interrupt Capability

The BLC-80/24 and 80/28 boards provide vectoring for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A-2 CPU and represent the four highest priority interrupts of the BLC-80/24 and 80/28 boards. Requests are routed to the 8085A-2 interrupt inputs—TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority), each of which generates a call instruction to a unique address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5:2CH). An 8085A-2 JMP instruction at each of these addresses then provides linkage to interrupt service routines located independently anywhere in memory. All interrupt inputs with the exception of the trap interrupt may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A-2 CPU. The 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, BLX bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32 or 64-byte block may be located to begin at any 32 or 64-byte boundary in the 65,536-byte memory space. A single 8085a-2 JMP instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Autorotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based on sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Interrupt Request Generation

Interrupt requests may originate from 23 sources. Two jumper selectable interrupt requests can be generated by each BLX EXPANSION MODULE. Two jumper selectable interrupt requests can be automatically generated by each programmable peripheral interface when a byte of information is ready

to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Three jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receiver channel buffer is full), a character is ready to be transmitted (i.e., the USART is ready to accept a character from the CPU), or when the transmitter is empty (i.e., the USART has no character to transmit). A jumper selectable request can be generated by each of the programmable timers. Nine interrupt request lines are available to the user for direct interface to user designated peripheral devices via the MULTIBUS system bus. A power-fail signal can also be selected as an interrupt source.

Power-Fail Control

A power-fail interrupt may be detected through the AC-low signal generated by the power supply. This signal may be configured to interrupt the 8085A-2 CPU to initiate an orderly power down instruction sequence.

MULTIBUS System Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using NATIONAL Series/80 MULTIBUS system compatible expansion boards. With the bank select option, memory may be expanded to 128KB by adding user specified combinations of RAM boards (BLC-8064), EPROM boards (BLC-464), or combination boards. Input/output capacity may be increased by adding digital I/O (BLC-5191) and analog I/O (BLC-8737) expansion boards. Mass storage capability may be achieved by adding single or double density diskette (BLC-8222) or hard disk controllers (BLC-8225) as subsystems. Expanded communication needs can be handled by communication controllers (BLC-8538). Modular expandable backplanes and card cages (BLC-604) are available to support multiboard systems.

System Support Real-Time Software

The BLMX-80 executive, which contains all major real-time facilities including priority-based system resource allocation, intertask communication and control, interrupt driven control for standard I/O devices, and interrupt handling occupies 2K bytes of memory which can be stored on-board in EPROM. Optional linkable and relocatable modules for console control (CRT or TTY), disk file system, and analog subsystems are provided with the BLMX-80 package. These facilities eliminate the need for users to design and implement application specific executives, greatly simplifying application design and reducing development time and risk.

System Monitor Firmware

The BLC-80/24, 28 system monitor is available in pre-programmed PROMs. This comprehensive monitor includes facilities to load, execute, and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Routines are included to load or save programs using paper tape. It permits the insertion of break points to facilitate debugging. Programs may be executed starting at any location, or single stepped. A baud rate search capability is built in which automatically determines the baud rate of the terminal being used at initialization.

System Development Capability

The development cycle of BLC-80/24 and 80/28 based products may be significantly reduced using NATIONAL's system development tools available today. The STARPLEX™ family of compatible microcomputer development systems provides a range of capability from a low cost disk-based edit debug workstation to a high performance, fully compatible hard-disk-based software development system. Also, a unique in-circuit emulator (ISE-8085 Emulator Pkg)™ option provides the capability of developing and debugging software directly on the BLC-80/24 and 80/28 boards.

SPECIFICATIONS

Word Size

Instruction—8, 16, or 24 bits
Data—8 bits

Cycle Time

Basic Instruction Cycle

826 nsec (4.84 MHz operating frequency)
1.65 μsec (2.42 MHz operating frequency)

NOTE:
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board EPROM

0-0FFF using 2758 (1 wait state)
0-1FFF using 2716 (1 wait state)
0-3FFF using 2732 (1 wait state)
using 2732A (no wait states)
0-7FFF using 2764A (no wait states)

On-Board RAM

3000-3FFF for BLC-80/24
2000-3FFF for BLC-80/28

NOTE:
Default configuration—may be reconfigured to top end of any 4K boundary.

Programming Capability

PL/M-80—National's high level system programming language, PL/M, is also available as a resident Starplex™ microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time then assembly language programs.

Memory Capacity

On-Board EPROM

32K bytes (sockets only)
May be added in 1K (using 2758s), 2K (using 2716), 4K (using 2732), or 8K (using 2764) byte increments.

On-Board RAM

4K bytes for BLC-80/24 and 8K bytes for BLC-80/28. May be disabled using PROM ENABLE via I/O port and jumper option, resulting in off-board RAM overlay capability.

I/O Addressing

On-Board Programmable I/O

Device	I/O Address
8255A No. 1	
Port A	E4
Port B	E5
Port C	E6
Control	E7
8255A No. 2	
Port A	E8
Port B	E9
Port C	EA
Control	EB
8251A	
Data	EC, EE
Control	ED, EF
BLX Expansion Module	
MCS0	C0-C7
MCS1	C8-CF
BLX Expansion Module	
MCS0	F0-F7
MCS1	F8-FF

I/O Capacity

Parallel—48 programmable lines

Serial—1 transmit, 1 receive, 1 SID, 1 SOD

BLX EXPANSION—2 BLX EXPANSION CONNECTORS

Serial Communications Characteristics

Synchronous—5-8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous—5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Register Address (hex notation, I/O address space)

DE Baud rate register

NOTE:
Baud rate factor (16 bits) is loaded as two sequential output operations to same address DE_H).

Baud Rates

Output Frequency in kHz	Baud Rate (Hz)		
	Synchronous	Asynchronous	
153.6	—	÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Interrupts

Addresses for 8259A Registers (hex notation, I/O address space)

DA or D8 Interrupt request register
DA or D8 In-service register
DB or D9 Mask register
DA or D8 Command register
DB or D9 Block address register
DA or D8 Status (polling register)

NOTE:
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt levels routed to 8085A-2 CPU automatically vector the processor to unique memory locations:

Interrupt Input	Memory Address	Priority	Type
TRAP	24	Highest	Non-maskable
RST 7.5	3C		Maskable
RST 6.5	34		Maskable
RST 5.5	2C	Lowest	Maskable

Timers

Register Addresses (hex notation, I/O address space)

DF Control register
DC Timer 0
DD Timer 1
DE Timer 2

NOTE:
Timer counts loaded as two sequential output operations to same address as given.

Input Frequencies

Reference: 1.0752 MHz ±0.1% (0.930 μsec period, nominal)

Event Rate: 1.1 MHz max.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min.	Max.	Min.	Max.
Real-Time Interrupt	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
Programmable One-Shot	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-Wave Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Software Triggered Strobe	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
Hardware Triggered Strobe	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs

NOTE:
Input frequency to timers is 1.0752 MHz (default configuration).

Interfaces

MULTIBUS—All signals TTL compatible

BLX Bux—All signals TTL compatible

Parallel I/O—All signals TTL compatible

Serial I/O—RS232C compatible, configurable as a data set or data terminal

Timer—All signals TTL compatible

Interrupt Requests—All TTL compatible

System Clock (8085A-2 CPU)

4.84 or 2.42 MHz ±0.1% (jumper selectable)

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors*
MULTIBUS System Bus	86	0.156	ELFAB BS1562043PBB Viking 2KH43/9AMK12 Soldered PCB Mount EDAC 337086540201 ELFAB BW1562D43PBB EDAC 337086540202 ELFAB BW1562A43PBB Wire Wrap
Auxiliary Bus	60	0.100	EDAC 345060524802 ELFAB BS1020A30PBB EDAC 345060540201 ELFAB BW1020D30PBB Wire Wrap
BLX Bus (2)	36	0.100	Viking 002101-0000C
Parallel I/O (2)	50	0.100	3M 3415-001 Flat Crimp GTE Sylvania 6AD01251A1DD Soldered
Serial I/O	26	0.100	AMP 15837151 EDAC 345026520202 PCB Soldered 3M 3462-0001 AMP 88373-5 Flat Crimp

***NOTE:**
Connectors compatible with those listed may also be used.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

I/O Drivers—The following line drivers and terminators are all compatible with the I/O driver sockets on the BLC-80/24 and 80/28 Boards:

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I = inverting; NI = non-inverting; OC = open collector.

Ports E4 and E8 have 32 mA totem-pole drivers and 1K terminators.

I/O Terminators—220Ω/330Ω divider or 1 kΩ pullup.

Electrical Characteristics

DC Power Requirements

Configuration	Current Requirements			
	V_{CC} = +5V ±5% (max)	V_{DD} = +12V ±5% (max)	V_{BB} = −5V ±5% (max)	V_{AA} = −12V ±5% (max)
Without EPROM[1]	3.34A	40 mA	—	20 mA
RAM Only[2]	0.14A	—	—	—
With BLC 530[3]	3.34A	140 mA	—	120 mA
With 8K EPROM[4] (using 2716)	4.43A	40 mA	—	20 mA
With 16K EPROM[4] (using 2732)	4.71A	40 mA	—	20 mA
With 32K EPROM[4] (using 2764)	4.71A	40 mA	—	20 mA

NOTES:
1. Does not include power for optional EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus.
3. Does not include power for optional EPROM, I/O drivers, and I/O terminators. Power for iSBC 530 Adapter is supplied via serial port connector.
4. Includes power required for four EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Address	Tri-State	32
Commands	Tri-State	32

Physical Characteristics

Width—12.00 in. (30.48 cm)
Height—6.75 in. (17.15 cm)
Depth—0.50 in. (1.27 cm)
Weight—12.64 oz. (354 gm)

Environmental Characteristics

Operating Temperature—0°C to 55°C

ORDERING INFORMATION

Part Number	Description
BLC-80/24	Board Level Computer w/4KB RAM
BLC-80/28	Board Level Computer w/8KB RAM
BLC-920	System Monitor Firmware

Reference Manual

BLC-80/24M—Hardware Reference Manual for BLC-80/24

BLC-80/28M—Hardware Reference Manual for BLC-80/28

BLC-920M—System Monitor Firmware Manual

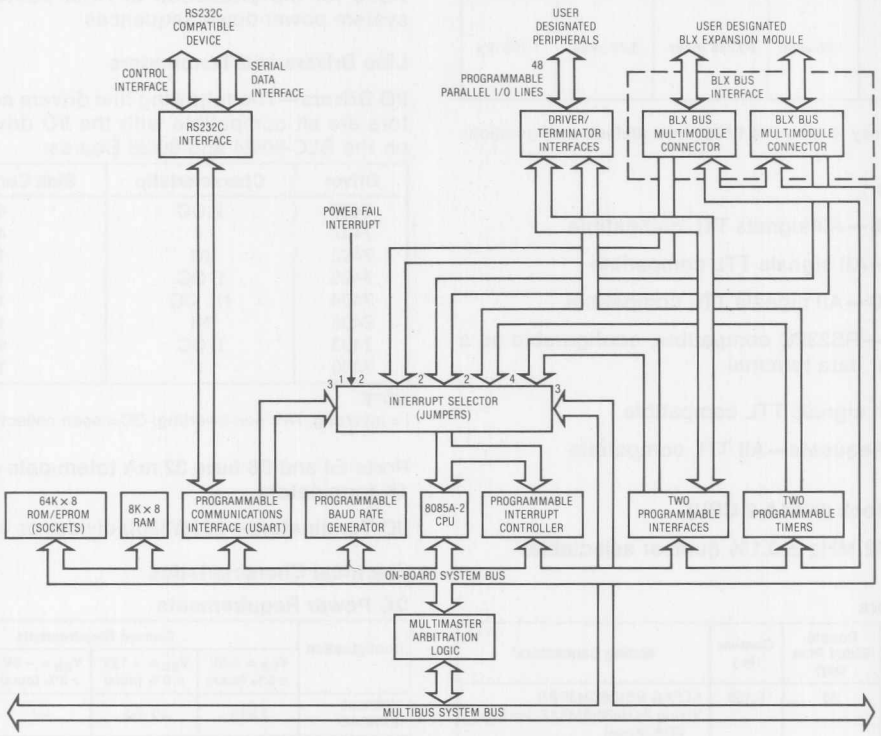
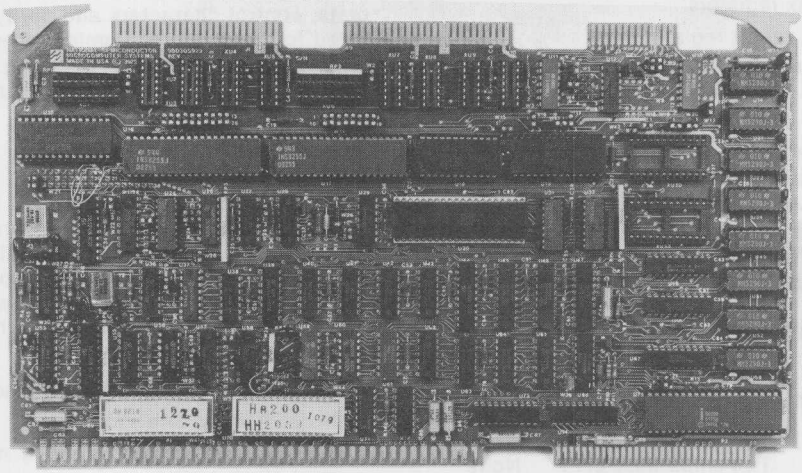


Figure 1. 80/28 Board Level Computer Block Diagram

National Semiconductor

BLC-80/316
Series/80 Board Level Computer



- **Z-80A Microprocessor**
- **Dual Port RAM**
- **Sockets for up to 8K PROM**
- **Multiple Processor Arbitration Implemented In Hardware**
- **ROM/RAM "Shadowing" Capability under Software Control**
- **3 Counter/Timers**
- **RS232C Serial Interface**
- **16K On-Board Memory**
- **9 Levels of Vectored Interrupts**
- **RAM Battery Back-Up Logic Fully Implemented**
- **48 Programmable Parallel I/O Lines**
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**

Product Overview

The BLC-80/316 is a single-board computer featuring the Z-80A CPU. The Z-80A is an enhancement of the 8080A, capable of performing 158 instructions, addressing 64K bytes of memory and 256 I/O ports. Included on the BLC-80/316 are 16K of dynamic RAM with dual port control. Sockets are available for up to 8K ROM, serial and parallel I/O, and extensive interrupt capability.

Functional Descriptions

Central Processor

- CPU: Z-80A Microprocessor
- 16-Bit address bus
- 8-Bit data word
- Instruction word — 8, 16, 24 bits
- 3.69 MHz clock rate (1.08 microsecond instruction cycle)
- Full object code software compatibility with the 8080A
- 158 Instruction set (47 more than 8080A)
- Type Instructions
  - — Load and exchange
  - — Block test and search
  - — Arithmetic and logical
  - — Rotate and shift
  - — Bit manipulation (set, reset and test)
  - — Jump, call and return
  - — Input/Output
  - — Basic CPU control

Z80A® is a registered trademark of Zilog Corp.

- 22 Registers
  - — Main registers A (accumulator), B, C, D, E, F (flags), H, L
  - — Alternate Registers A' (accumulator) B', C', D', E', F' (flags), H', L'
  - — Program counter
  - — Stack pointer
  - — Two index registers
  - — Interrupt vector register
  - — Refresh register

There are two types of memory on the BLC-80/316:

- PROM/ROM
  - — Two sockets are available for up to 8K in 1K, 2K, and 4K byte increments. A ROM shadow feature is incorporated allowing ROM to be made to "disappear", and replaced by system RAM, under software control.

Table I. PROM/ROM Types and Addresses

				Addresses	
ROM	**PROM**	**Memory**	**/Chip**	**Allowed**	**Unavailable**
2308	2708	1K	One chip	0000-03FF	0400-07FF
			Two chips	0000-07FF	None
	2758	1K	One chip	0000-03FF	0400-07FF
			Two chips	0000-07FF	None
2316	2716	2K	One chip	0000-07FF	0800-0FFF
			Two Chips	0000-0FFF	None
2332	2732	4K	One chip	0000-0FFF	1000-1FFF
			Two chips	0000-1FFF	None

- RAM
  - — The shared memory is locatable on 8K or 16K boundaries anywhere within a 64K page within a 1 MB range. The shared memory address need not be the same as the private memory.
  - — There are hardware provisions to allow for the dedication of 8K or all 16K of the on-board RAM to the on-board CPU via jumpers. If 8K is private, it can be located on any 8K boundary up to 64K (16K boundaries if 16K private).
  - — RAM is separated from the system bus arbitrator logic between the Z-80A and the board requesting access to on-board RAM. The Z-80A is always given priority to allow for maximum on-card throughput.

Input/Output

Parallel I/O

Two INS8255 programmable peripheral interface circuits provide a total of 48 I/O lines which can be configured by software into any combination of unidirectional/bidirectional I/O ports. Sockets are provided on the board to allow selection of drivers and terminators appropriate for each application. All I/O lines are interfaced using a pair of 50 contact edge connectors for mating with cables.

Serial I/O

One INS8251 Universal Synchronous/Asynchronous Receiver/Transmitter provides the serial I/O port with programmable communications rates, data formats, control characters and parity. Logic is provided for detection of framing, overrun and parity errors, as well as double buffering. The serial I/O port provides RS232C signals interfaced via a 26 contact edge connector.

Timers

One 8253 programmable interval timer provides three programmable 16-bit counters. One is used as a baud rate generator for the serial I/O port, and the other two are used as general purpose BCD or binary 16-bit counters, which can be cascaded into one 32-bit counter. Each clock has up to six software selectable functions:

- Interrupt on termination of a specified count
- Programmable one-shot
- Rate generator based upon a multiple of the input clock period
- Square wave rate generator (counter 2 should be programmed in this mode)
- Software triggered strobe
- Hardware triggered strobe
- Event counter (using external signal to drive clock input)

Input Frequencies:	Reference — 1.0752 MHz ± 1.1% Event rate — 1.1 MHz maximum
Timing Intervals:	Frequency variation from 25 kHz to 537.61 kHz.
Output Frequencies:	Variable time intervals from 1.86 microseconds to 1.109 hours

Interrupt System

Interrupts to the Z-80A are handled in two ways. The first, simplest, is the NMI, or non-maskable interrupt directly to the Z-80A. This interrupt causes the Z-80A to execute a restart instruction at location 0066H.

The second method of handling interrupts with the BLC-80/316 makes use of the 8259 Programmable Interrupt Controller (PIC). The PIC communicates with the Z-80A across an 8-bit data bus and is addressed as two ports.

The 8259 PIC accepts up to 8 interrupt inputs and provides an interrupt signal to the Z-80A. When the Z-80A recognizes the interrupt, the PIC generates a call instruction and 16-bit starting address for the Z-80A interrupt service routine. Four different operating modes can be programmed to handle interrupt priority.

System Bus Arbitration

The Series/80 system bus allows multiple devices to transfer data on a common bus.

The BLC-80/316 takes advantage of this bus by using the H8218 bus controller chip. Several options have been implemented.:

- Option to request only when needed
- Option to run in override mode by jumpering a bus controller input to a port D7 bit
- Option to remove BPRO/ from bus (for parallel resolution circuitry).

The system bus will be able to make use of the CBRQ command. This open collector output "OR ties" several masters together indicating one or multiple masters are requesting the bus. Used for a parallel resolution network, the H8218 will handle up to 6 bus masters in a serial resolution network, and up to 16 in a parallel configuration.

Power Fail and Memory Protect

Capabilities on the BLC-80/316 for power failure consist of a battery back-up bus, power fail interrupt input, power fail status input, and memory protect input.

BLC-8930 System Firmware

The BLC-8930 system monitor is available in a preprogrammed MM2716 PROM. This comprehensive monitor includes facilities to load, execute, and debug programs based on the Z-80A CPU. The monitor allows the user to examine and modify any RAM memory location or CPU register. It also allows for the loading of HEX data to memory from paper tape. The debugging tools allow you to move blocks of data in memory, insert breakpoints, and initiate execution of user programs. The monitor incorporates a search to establish the baud rate at which the CRT/TTY are running. The commands supported by the BLC-8930 System Monitor are:

A — ASCII display
D — Display contents of memory
F — Find data in memory
G — Execute program and/or set breakpoints
H — Hexadecimal arithmetic
I — Insert to memory
M — Move memory
N — Single step
O — Output data to port
R — Read hex tape
S — Substitute memory
T — Type input ports
X — Examine and modify CPU registers

Specifications

Microprocessor

CPU — Z-80A

Data Word — 8 bits

Instruction Word — 8, 16, 24 bits

Cycle Time — 1.08 microseconds (minimum instruction cycle)

System Clock — 3.69 MHz ± 0.1%

Registers — 14 General Purpose, 8-bit registers
Two 8-bit accumulators
Two 8-bit index registers
One 8-bit interrupt vector register
One 8-bit refresh register
One 16-bit program counter
One 16-bit stack pointer

Number of Instructions — 158

Address Capacity — 64K bytes

Memory

RAM — 16K bytes on-board

ROM — Sockets for up to 8K bytes on-board

Expansions — (ROM/PROM/EPROM) Memory boards in any mix of RAM and ROM up to 1 megabyte maximum

Access Time — 271 nanoseconds (maximum)

Input/Output

Interrupts — 9 level hardware vectored interrupts
Programmable masking
4 priority modes

Parallel — 48 programmable I/O Lines latched, unlatched, strobed modes
4- and 8-bit parallel configuration
Optional line drivers and terminators
TTL compatible

Compatible I/O Driver Modules (I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Type	Output	Current (mA)
7438	I,OC,HV	48
7437	I	48
7432	NI	16
7426	I,OC,HV	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Compatible I/O Terminator Modules — BLC-901 220/330 ohm Divider
BLC-902 1K ohm Pull-Up

Serial — Programmable full data set control
Double buffered RS232C compatible

Synchronous Mode — 5-8-bit character,
Internal/external synchronization
automatic SYNC insertion
SYNC search 75-9600 baud rate

Asynchronous Mode — 5-8-bit character
1, 1½, or 2 stop bits
False start bit detect
1760-38400 baud
Break character generation

System Bus — Multiple bus master capability for up to 6 masters, expandable to 16 masters with additional priority network. All address, data and control signals are Tri-State

Interval Timer (Clocks)

Clocks — 3 programmable

Size — 16 bits

Interval — 1.86 microseconds to 1.109 hours

Frequency Variation — 25 kHz to 537.61 kHz

Connectors

System Bus — 86-contact double-sided card cage edge connector on 0.156-inch centers

Auxiliary (Battery Back-Up) — 60-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
CDC VPB01B30A0042
AMP PES-14559
TI H311130

Parallel I/O — 50-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

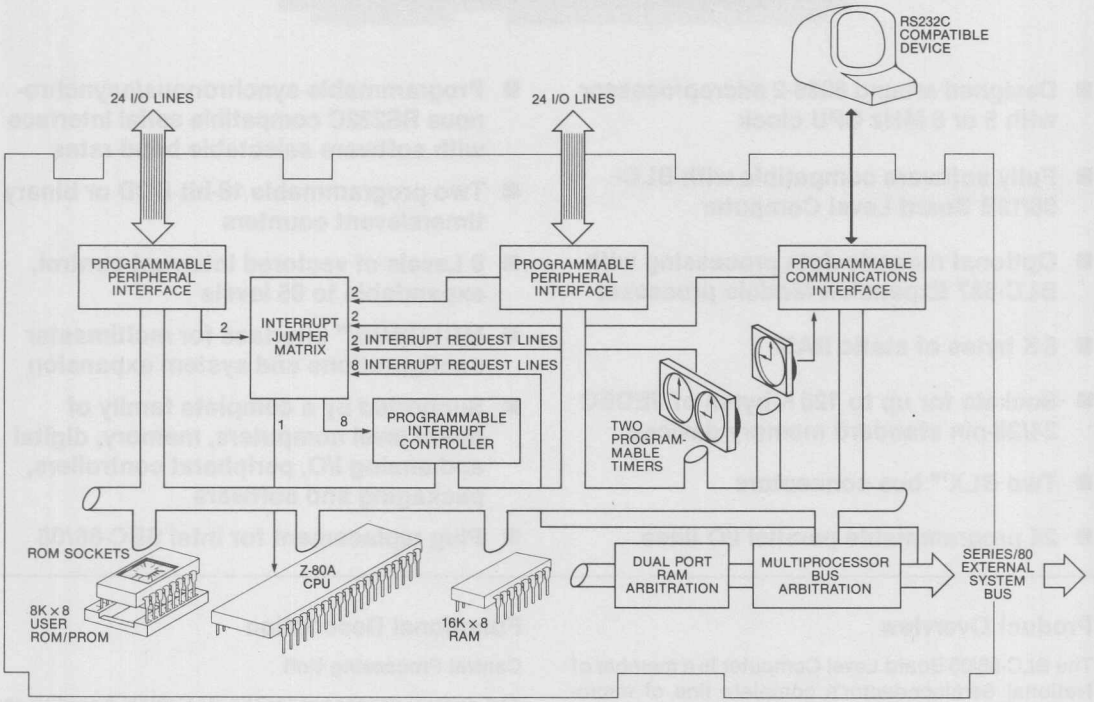
Serial I/O — 26-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power	**VDC**	**Normal**	**Battery**
	+5V	4.9A	0.56A
	−5V	0.18A	—
	+12V	0.35A	—
	−12V	0.02A	—

Environmental Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical			
	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	17 oz.	(482 gm)

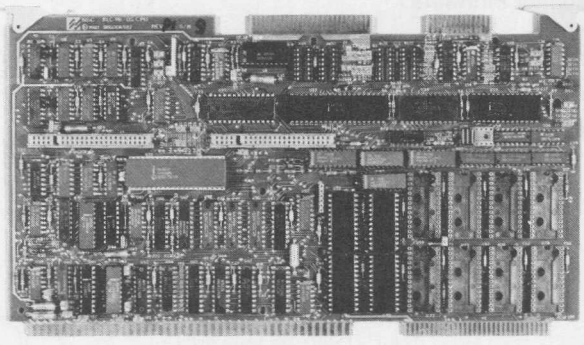
	Includes CPU, 16K bytes of dual port RAM, sockets for 84 bytes of PROM/ROM, 48 parallel I/O Lines, and RS232C port	420306218-001	BLC-8930 User's Manual
BLC-8930	System Monitor Firmware		



BLC-80/316 Diagram

National Semiconductor

BLC-86/05
Board Level Computer



- **Designed around 8086-2 microprocessor with 5 or 8 MHz CPU clock**
- **Fully software compatible with BLC-86/12B Board Level Computer**
- **Optional numeric data processing with BLC-337 Expansion Module processor**
- **8 K bytes of static RAM**
- **Sockets for up to 128 K bytes of JEDEC 24/28-pin standard memory devices**
- **Two BLX™ bus connectors**
- **24 programmable parallel I/O lines**
- **Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rates**
- **Two programmable 16-bit BCD or binary timers/event counters**
- **9 Levels of vectored interrupt control, expandable to 65 levels**
- **MULTIBUS™ interface for multimaster configurations and system expansion**
- **Supported by a complete family of board level computers, memory, digital and analog I/O, peripheral controllers, packaging and software**
- **Plug replacement for Intel SBC-86/05**

Product Overview

The BLC-86/05 Board Level Computer is a member of National Semiconductor's complete line of microcomputer systems which take full advantage of the latest technology to provide economical, computer-based solutions for test systems, industrial control, and OEM applications. The BLC-86/05 board is a complete computer system on a single 6.75 × 12.00-in. printed circuit board. The CPU, system clock, read/write memory, non-volatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The large control storage capacity makes the BLC-86/05 board ideally suited for control-oriented applications such as process control, instrumentation, industrial automation, and many others.

Functional Description

Central Processing Unit

The central processor for the BLC-86/05 board is an 8086-2 microprocessor. A clock rate of 8 MHz is supported with a jumper selectable option of 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers, all accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages, as well as assembly language.

Instruction Set

The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the BLC-337 Numeric Data Processor expansion module extends the 8086-2 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

Architectural Features

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 750 ns minimum instruction cycle to 250 ns for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, intermodule communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X*
	4	X		X			X*

***Note:** Part of port 3 must be used as a control port when either port 1 or port 2 is used as a latched and strobed input or a latched and strobed output port, or port 1 is used as a bidirectional port.

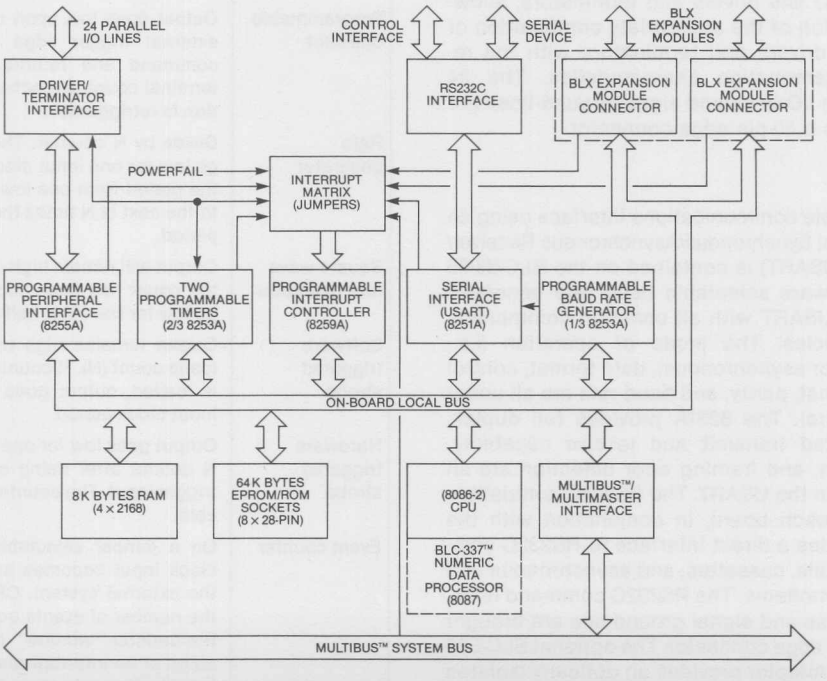


Figure 1. BLC-86/05 Block Diagram

register maps 64 K bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

Memory Configuration

The BLC-86/05 microcomputer contains 8 K bytes of high-speed static RAM on-board. All on-board RAM is accessed by the 8086-2 CPU with no wait states, yielding a memory cycle time of 500 ns.

In addition to the on-board RAM, the BLC-86/05 board has eight 28-pin sockets, configured to accept JEDEC 24/28-pin standard memory devices. Up to 128 K bytes of EPROM are supported in 16 K-byte increments with 27128 EPROMs. Up to 32 K bytes of EPROM with 8 K-byte increments is provided by using 2732 devices, and 16 K bytes are supported by 2716 EPROMs with 4 K-byte increments. Other JEDEC standard pinout devices are also supported, including byte-wide static and pseudo static RAMs.

Parallel I/O Interface

The BLC-86/05 Board Level Computer contains 24 programmable parallel I/O lines implemented using an 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Serial I/O

A programmable communications interface using an 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the BLC-86/05 board. A software selectable baud rate generator provides the USART with all common communications frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector. The optional BLC-530 Current Loop Adapter provides an optically isolated interface from the BLC-86/05 serial interface for those devices requiring a 20 mA current loop interface, such as teletypewriters.

Programmable Timers

The BLC-86/05 board provides three independent, fully-programmable 16-bit interval timers/event counters utilizing an 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8253 provides the programmable baud rate generator for the BLC-86/05 board RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

BLX™ Expansion Modules for On-Board Expansion

Two 8/16-bit BLX Expansion Module connectors are provided on the BLC-86/05 microcomputer. Through these connectors, additional on-board I/O functions may be added. BLX Expansion Modules optimally support functions provided by VLSI peripheral components such as additional parallel (BLX-350) and serial I/O (BLX-351), analog I/O (BLX-321), floppy disk controllers (BLX-218), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS™ form factor compatible boards. The BLX connectors on the BLC-86/05 provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. BLX Expansion Module boards designed with 8-bit data paths and using the 8-bit BLX connector are also supported on the 86/05 microcomputer. A broad range of BLX Expansion Module options are available in this family from National Semiconductor. Custom BLX modules may also be designed for use on the BLC-86/05 board using the BLX-391 prototyping module.

MULTIBUS System Bus and Multimaster Capabilities

Overview

The MULTIBUS system bus is an industry standard microcomputer bus structure. Both 8 and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards (BLC-0512), EPROM boards (BLC-464), or combination boards (BLC-519). Input/output capacity may be added with digital I/O and analog I/O (BLC-8737) expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers (BLC-8224), or hard disk controllers (BLC-8225). Modular expandable backplanes and card cages (BLC-604) are available to support multiboard systems.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the BLC-86/05 board provides full MULTIBUS arbitration control logic. This control logic allows up to 6 BLC-86/05 boards or other bus masters, including Series/80 family MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Interrupt Capability

The BLC-86/05 board provides 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Interrupt Request Generation

Interrupt requests to be serviced by the BLC-86/05 board may originate from 24 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the BLC-635 and BLC-665 power supply or equivalent, to initiate an orderly shutdown of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS™ interface	Requests from MULTIBUS resident peripherals or other CPU boards	8; may be expanded to 64 with slave 8259A PICs on MULTIBUS boards
8255A Programmable Peripheral Interface	Signals input buffer full or output buffer empty; also BUS INTR OUT general purpose interrupt from driver/terminator sockets	3
8251A USART	Transmit buffer empty and receive buffer full	2
8253 Timers	Timer 0, 1 outputs; function determined by timer mode	2
BLX connectors	Function determined by BLX MULTIMODULE board	4 (2 per BLX connector)
Bus fail safe timer	Indicates addressed MULTIBUS resident device has not responded to command within 6 ms	1
Power fail interrupt	Indicates AC power is not within tolerance	1
Power line clock	Source of 120 Hz signal from power supply	1
External interrupt	General purpose interrupt from auxiliary (P2) connector on backplane	1
BLC-337 MULTIMODULE™ Numeric Data Processor	Indicates error or exception condition	1

System Monitor Firmware

The BLC-8957 system monitor is available in pre-programmed PROMS. This comprehensive monitor includes facilities to load, execute, and debug programs. The monitor allows the user to examine and modify any RAM memory location or CPU register. Routines are included to load or save programs using paper tape. It permits the insertion of breakpoints to facilitate debugging. Programs may be executed starting at any location, or singlestepped. A baud rate search capability is built in which automatically determines the baud rate of the terminal being used at initialization.

Specifications

Word Size

Instruction — 8, 16, 24, or 32 bits

Data — 8, 16 bits

System Clock 5.00 MHz or 8.00 MHz ±0.1% (jumper selectable)

Cycle Time

Basic Instruction Cycle

At 8 MHz — 750 ns

250 ns (assumes instruction in the queue)

At 5 MHz — 1.2 μs

400 ns (assumes instruction in the queue)

Note: Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Memory Cycle Time

RAM — 500 ns (no wait states)

EPROM — Jumper selectable from 500 ns to 875 ns

Memory Capacity/Addressing

On-Board EPROM

Device	Total Capacity	Address Range
2716	16 K bytes	$FC000\text{-}FFFFF_H$
2732	32 K bytes	$F8000\text{-}FFFFF_H$
2764	64 K bytes	$F0000\text{-}FFFFF_H$

Note: BLC-86/05 EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMs.

On-Board RAM

8 K bytes — $0\text{-}1FFF_H$

I/O Capacity

Parallel — 24 programmable lines using one 8255A.

Serial — Programmable port using one 8251A

BLX™ Expansion — 2 BLX Expansion Module connectors

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection

Baud Rates

Frequency (KHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

Note: Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Timers

Input Frequencies — Reference: 2.46 MHz ±0.1% (0.041 μs period, nominal); or 153.60 KHz ±0.1% (6.51 μs period, nominal)

Note: Above frequencies are user selectable.

Event Rate: 2.46 MHz max.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min.	Max.	Min.	Max.
Real-time Interrupt	1.63 μs	427.1 ms	3.26s	466.50 min.
Programmable one-shot	1.63 μs	427.1 ms	3.26s	466.50 min.
Rate generator	2.342 Hz	613.5 KHz	0.000036 Hz	306.8 KHz
Square-wave rate generator	2.342 Hz	613.5 KHz	0.000036 Hz	306.8 KHz
Software triggered strobe	1.63 μs	427.1 ms	3.26s	466.50 min.
Hardware triggered strobe	1.63 μs	427.1 ms	3.26s	466.50 min.
Event counter	—	2.46 MHz	—	—

Interfaces

MULTIBUS™ — All signals TTL compatible

BLX™ BUS — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — RS232C compatible, configurable as a data set or data terminal

Timer — All signals TTL compatible

Interrupt Requests — All signals TTL compatible

Connectors

Interface	Double-Sided Pins (qty)	Centers (inches)	Mating Connectors
MULTIBUS System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
BLX Bus			
8-Bit Data	36	0.1	VIKING 002101-0000C
16-Bit Data	44	0.1	VIKING 002101-0006
Parallel I/O (2)	50	0.1	3M 3415-000 Flat or TI H312125 Pins
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

Line Drivers and Terminators

I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the BLC-86/05 board

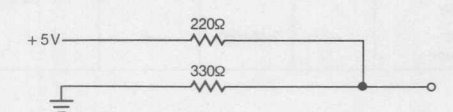
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Notes: I = inverting; NI = non-inverting; OC = open collector.

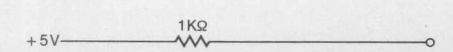
Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 KΩ terminators

I/O Terminators — 220Ω/330Ω divider or 1 KΩ pullup

220Ω/330Ω (BLC-901 Option)



1 KΩ (BLC-902 Option)



MULTIBUS Drivers

Function	Characteristic	Sink Current (mA)
Data	TRI-STATE®	50
Address	TRI-STATE	50
Commands	TRI-STATE	32
Bus Control	Open Collector	20

Physical

Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.70 in.	(1.78 cm)
Weight	14 oz.	(388 gm)

Electrical

DC Power Requirements

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM[1]	4.7A	25 mA	23 mA
RAM only[2]	120 mA		
With 16K EPROM[3] (using 2716)	5.0A	25 mA	23 mA
With 32K EPROM[3] (using 2732)	4.9A	25 mA	23 mA
With 64K EPROM[3] (using 2764)	4.9A	25 mA	23 mA

Notes:

1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Environmental Temperature: 0°C to 55°C

Humidity: 0 to 90% (noncondensing)

Ordering Information

BLC-86/05 Board Level Computer

BLC-8957 System Monitor Firmware

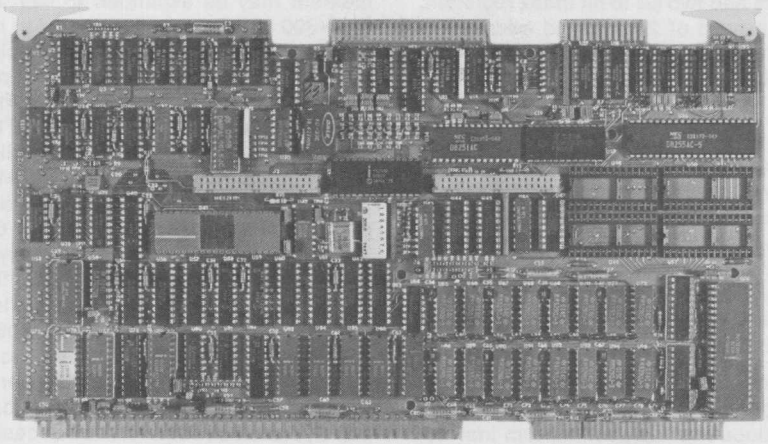
Documentation

BLC-86/05M BLC-86/05 Hardware Reference Manual

BLC-8957M System Monitor Firmware Manual

National Semiconductor

BLC-86/12B
Board Level Computer



- 8086 16-bit microprocessor central processing unit
- 32 K bytes of dual-port read/write memory expandable on-board to 64 K bytes with on-board refresh
- Sockets for up to 32 K bytes of read only memory
- System memory expandable to 1 megabyte
- 24 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators
- Programmable synchronous/ asynchronous RS232C compatible serial interface with software selectable baud rates
- Two programmable 16-bit BCD or binary timers/event counters
- Two BLX connectors for on-board I/O expansion
- 9 levels of vectored interrupt control, expandable to 65 levels
- Auxiliary power bus and power fail interrupt control logic for read/write memory battery backup
- Multibus™ interface for multimaster configurations and system expansion
- Dual port RAM with lock-out capability for system security
- Compatible with Series/80 family board level computers, memory, digital and analog I/O, and peripheral controller boards

Product Overview

The BLC-86/12B Board Level Computer is a member of National Semiconductor Corporation's complete line of OEM microcomputer systems which take full advantage of the latest LSI technology to provide economical, self-contained, computer-based solutions for OEM applications. The BLC-86/12B board is a complete computer system on a single 6.75 × 12.00-inch printed circuit card. The CPU, system clock, read/write memory, non-volatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. Full Multibus interface logic is included to offer compatibility with the Series/80 family of board level computers, expansion memory options, digital and analog I/O expansion boards and peripheral controllers. Two BLX bus compatible connectors are also provided for incremental on-board expansion with the growing line of BLX expansion modules from National Semiconductor Corporation.

Multibus is a trademark of Intel Corp.

Functional Description

Central Processing Unit

The central processor for the BLC-86/12B board is the 8086, a powerful 16-bit microprocessor. The architecture includes four (4) 16-bit byte addressable data registers and two (2) 16-bit index registers, all accessed by a total of 24 operand addressing modes for complex data handling and very flexible memory addressing.

Instruction Set — The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. The instruction set of the 8086 is a superset of the 8080A/8085A family and with available software tools, programs written for the 8080A/8085A can be easily converted and run on the 8086 processor.

Architectural Features — A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 1.22 μs minimum instruction cycle to 407 ns for queued instructions. The stack oriented architecture facilitates nested subroutines and co-routines, reentrant code and powerful interrupt handling. The memory expansion capabilities offer a 1 megabyte addressing range. This dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64 K bytes at a time and activation of a specified register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

Bus Structure

The BLC-86/12B microcomputer has three buses: an internal bus for communicating with on-board memory and I/O options (including BLX modules), the Multibus system bus for referencing additional memory and I/O options, and the dual-port bus which allows access to RAM from the on-board CPU and the Multibus system bus. Local (on-board) accesses do not require Multibus communication, making the system bus available for use by other Multibus masters (i.e., DMA devices and other board level computers transferring to additional system memory). This feature allows true parallel processing in a multiprocessor environment. In addition, the Multibus interface can be used for system expansion through the use of other 8- and 16-bit Series/80 computers, memory, and I/O expansion boards.

RAM Capabilities

The BLC-86/12B microcomputer contains 32 K bytes of dynamic read/write memory using 16 K-bit MM5290 RAMs. In addition, the on-board RAM complement may be expanded to 64 K bytes with the BLC-300 32 K byte RAM expansion module. Power for the on-board RAM and refresh circuitry may be optionally provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The BLC-86/12B board contains a dual port controller which allows access to the on-board RAM (32 K bytes, or 64 K bytes when the BLC-300 module is installed on the BLC-86/12B board) from the 8086 CPU, and from any other Multibus master via the system bus. The dual port controller allows 8- and 16-bit accesses from the Multibus system bus, while the on-board CPU transfers data to RAM over a 16-bit data path. Priorities have been established such that memory refresh is guaranteed by the on-board refresh logic and that the on-board CPU has priority over Multibus system bus requests for access to RAM. The dual port controller includes independent addressing logic for RAM access from the on-board CPU and from the Multibus system bus. The on-board CPU will always access RAM starting at location 00000_H. Address jumpers allow on-board RAM to be located starting on any 8 K byte boundary within a 1 megabyte address range for accesses from the Multibus system bus. In conjunction with this feature, the BLC-86/12B microcomputer has the ability to protect on-board memory from Multibus access to any contiguous 8 K byte segments (or 16 K byte segments with BLC-300 module).

These features allow multiprocessor systems to establish local memory for each processor and shared system (Multibus) memory configurations where the total system memory size (including on-board memory) can exceed 1 megabyte without addressing conflicts.

Dual Port Lock-Out Capability

The dual port RAM on the BLC-86/12B can be assigned exclusively to a controlling bus master during a critical period of time, e.g. Read-Modify-Write cycle. This happens when the dual port RAM is accessed by a controlling bus master which is overriding the bus (i.e., LOCK* is activated on the bus). The on-board CPU's request to the dual port RAM will be denied until LOCK* is removed. This feature provides system security for a system with dual port RAM without any software overhead or performance penalty.

Port	Lines (Qty.)	Input		Output		Bidirectional	Control
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

Note 1: Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input, or a latched and strobed output port, or port 1 is used as a bidirectional port.

EPROM/ROM Capablities

Four sockets are provided for up to 32 K bytes of nonvolatile read only memory on the BLC-86/12B board. EPROM/ROM may be installed in 2 K byte increments up to a maximum of 4 K bytes by using 2758 electrically programmable ROMs (EPROMs); in 4 K byte increments up to 8 K bytes by using 2716 EPROMs or 2316E masked ROMs; in 8 K byte increments up to 16 K bytes by using 2732 EPROMs or 2332A ROMs, or in 16 K byte increments up to 32 K bytes by using 2764 EPROMs. On-board EPROM/ROM is accessed via 16-bit data paths. System memory size is easily expanded by the addition of Multibus system bus compatible memory boards in the Series/80 product family.

Parallel I/O Interface

The BLC-86/12B single board computer contains 24 programmable parallel I/O lines implemented using the 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of undirectional input/output and bidirectional ports indicated in Table I.

Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the larger number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven or round cable (such as BLC-956).

Serial I/O

A programmable communications interface using the 8251A Universal Synchronous/Asynchronous Receiver Transmitter (USART) is contained on the BLC-86/12B board. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on the BLC-86/12B, in conjunction with the USART, provides a direct interface to terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26 pin edge connector that mates with RS232C compatible flat or round cable (such as BLC-955). The BLC-530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The BLC-530 unit may be used to interface the BLC-86/12B board to teletypewriters or other 20 mA current loop equipment.

Programmable Timers

The BLC-86/12B board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the 8253 Programmable Interval timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, or may be routed as inputs to the 8255A

Table II. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter terminal count	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

chip. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the BLC-86/12B board RS232C USART serial port. In utilizing the BLC-86/12B board, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table II. The contents of each counter may be read at any time during system operation with simple read operations for event counting. The applications and special commands are included so that the contents can be read "on the fly".

Multibus System Bus and Multimaster Capabilities

The Multibus system bus features asynchronous data transfers for the accommodation of devices with various transfer rates while maintaining maximum throughput. Twenty address lines and sixteen separate data lines eliminate the need for address/data multiplexing/demultiplexing logic used in other systems, and allow for data transfer rates up to 5 megawords/sec. A failsafe timer is included in the BLC-86/12B board which can be used to generate an interrupt if an addressed device does not respond within 5ms.

Multimaster Capabilities — The BLC-86/12B board is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the BLC-86/12B board provides full Multibus arbitration control logic. This control logic allows up to three BLC-86/12B boards or other bus masters, including Series/80 family Multibus compatible 8-bit board level computers, to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the Multibus system bus with the addition of an external priority network. The Multibus arbitration logic operates synchronously with a Multibus clock (provided by the BLC-86/12B board or optionally provided directly from the Multibus) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations and high speed peripheral control, but are by no means limited to these.

Interrupt Capability

The BLC-86/12B board provides 9 vectored interrupt levels. The highest level is the NMI (Non-maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt cannot be inhibited by software and is typically used for signalling catastrophic events (i.e., power failure). On servicing this interrupt, program control will be implicitly transferred through location 00008_H. The 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table III, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at

Table III. Programmable Interrupt Modes

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Autorotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

at any time during system operation. The PIC accepts interrupt requests from the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at 4 byte intervals. This 32-byte block may begin at any 32-byte boundary in the lowest 1K-bytes of memory, and contains unique instruction pointers and code segment offset values (for expanded memory operation) for each interrupt level. After acknowledging an interrupt and obtaining a device identifier byte from the 8259A PIC, the CPU will store its status flags on the stack and execute an indirect CALL instruction through the vector location (derived from the device identifier) to the interrupt service routine. In systems requiring additional interrupt levels, slave 8259A PIC's may be interfaced via the Multibus system bus to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Interrupt Request Generation — Interrupt requests may originate from 21 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. An additional interrupt request line may be jumpered directly from the parallel I/O driver terminator section. Four jumper selectable interrupt request lines from the BLX connectors are provided on the BLC-86/12B. Eight prioritized interrupt request lines allow the BLC-86/12B board to recognize and service interrupts originating from peripheral boards interfaced via the Multibus system bus. The Multibus fail safe timer can also be selected as an interrupt source.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the BLC-635 and BLC-665 Power Supply or equivalent.

On-Board Expansion Capabilities

Two BLX connectors are provided on the BLC-86/12B for on-board I/O and functional expansion. These connectors accept BLX expansion modules which are small boards interfaced directly to the CPU bus. This approach gives the user ultimate flexibility to enhance his system with minimum incremental cost and maximum system performance.

System Expansion Capabilities

Memory and I/O capacity may be expanded, and additional functions added, by using Multibus (or IEEE-796 Bus) compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

BLC-8957 System Monitor Firmware

The BLC-8957 system monitor is available in four preprogrammed MM2716 PROMs. This comprehensive monitor includes facilities for communications over either the serial port, or the parallel port (using an adapter board which is supplied with the BLC-8957). The user has the utilities to load, execute, and debug programs based on the 8086 CPU. The BLC-8957 allows the user to upload/download files on either the serial or parallel interfaces, examine and/or modify memory and CPU registers, move and compare blocks of memory, and control I/O. The

debugging tools allow the insertion of breakpoints, single stepping, locating a byte/word anywhere in memory, and provides hex math. The BLC-8957 incorporates a "search" to establish the baud rate of any serial device on either the serial or parallel interfaces. The commands supported by the system monitor are:

C — Compare two blocks of memory

D — Display contents of block of memory

F — Find a byte/word in block of memory

G — Start execution optionally with breakpoints

H — Perform hexadecimal addition and subtraction on two numbers

I — Input and display a byte/word

M — Move block of memory to another location

N — Single step with optional iterative count

O — Output a byte/word

R — Down load a binary object file from serial or parallel port

S — Display and/or modify memory locations

W — Up load a binary object file to serial or parallel port

X — Examine and/or modify CPU registers

Control-Z — Switch between serial and parallel ports and/or change the baud rate.

Specifications

Word Size

Instruction — 8, 16, 24, or 32 bits

Data — 8, 16 bits

Cycle Time

Basic Instruction Cycle — 1.22 μs-407 ns (assumes instruction in the queue)

Note: Basic instruction cycle is defined as the fastest instruction cycle time (i.e., two clock cycles)

Memory Capacity

On-Board ROM — 32K bytes (sockets only)

On-Board RAM — 32K bytes; expandable to 64K bytes with BLC-300 RAM expansion module

Off-Board Expansion — Up to 1 MB in user specified combinations of RAM, ROM, and EPROM

Note: ROM may be added in 2 K, 4 K, 8 K, or 16 K byte increments

Memory Addressing

On-Board EPROM/ROM — $FF000-FFFFF_H$ (using 2716 EPROMs or 2316 ROMs); $FC000-FFFFF_H$ (using 2732 EPROMs or 2332A ROMs); $F8000-FFFFF_H$ (using 2764 EPROMs).

On-Board RAM — 32 K bytes of dual port RAM. Optionally expandable to 64 K bytes with BLC-300 RAM option.

CPU Access — 32 K bytes: $00000-07FFF_H$; 64 K bytes: $00000-0FFFF_H$.

Multibus Access — Jumper selectable for any 8 K-byte boundary, but not crossing a 128 K byte boundary. Access for 8 K, 16 K, 24 K or 32 K (16 K, 32 K, 48 K, 64 K with BLC-300 option) bytes may be selected for on-board CPU use only.

I/O Capacity

Parallel — 24 programmable lines using one 8255A.

Serial — 1 programmable line using one 8251A.

BLX — 2 BLX connectors

I/O Addressing On-board progammable I/O

	8255A				USART	
	1	2	3	Control	Data	Control
Address	C8	CA	CC	CE	D8 or DC	DA or DE

BLX I/O Expansion

Addresses for BLX I/O connectors — C1, C3, C5, C7, C9, CB, CD, CF: I/O device 0 on J3.

D1, D3, D5, D7, D9, DB, DD, DF: I/O device 1 on J3.

E1, E3, E5, E7, E9, EB, ED, EF: I/O device 0 on J4.

F1, F3, F5, F7, F9, FB, FD, FF: I/O device 1 on J4.

Note: All the BLX I/O devices are 8-bit wide.

Serial Communications Interface

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; break, character generation; 1, 1½ or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38,400	2400	600
19.2	19,200	1200	300
9.6	9,600	600	150
4.8	4,800	300	75
2.4	2,400	150	—
1.76	1,760	110	—

Note: Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Interrupts

Addresses for 8259A Registers (Hex notation I/O address space)

C0 or C4 Write — Initialization Command Word 1 (CW1) and Operation Control Words 2 and 3 (OCW2 and OCW3)

Read — Status and Poll Register

C2 or C6 Write — ICW2, ICW3, ICW4, OCW1 (Mask Register)

Read — OCW1 (Mask Register)

Note: Several registers have the same physical address; sequence of access and one data bit of control word determines which register will respond.

Interrupt Levels — 8086 CPU includes a non-maskable Interrupt (NMI) and a maskable interrupt (INTR). NMI interrupt is provided for catastrophic events such as power failure. NMI vector address is 00008. INTR interrupt is driven by on-board 8259A PIC, which provides 8-bit identifier of interrupting device to CPU. CPU multiplies identifier by four to derive vector address. Jumpers select interrupts from 21 sources without necessity of external hardware. PIC may be programmed to accommodate edge-sensitive or level-sensitive inputs.

Timers

Register Addresses (Hex notation, I/O address space)

D0 — Timer 0

D2 — Timer 1

D4 — Timer 2

D6 — Control register

Note: Timer counts are loaded as two sequential output operations to same address as given.

Input Frequencies

Reference — 2.46 MHz ± 0.1% (407 ns period, nominal); 1.23 MHz ± 0.1% (0.81 μs period, nominal); or 153.60 kHz ± 0.1% (6.51 μs period nominal).

Note: Above frequencies are user selectable.

Event Rate — 2.46 MHz max.

Note: All the BLX I/O devices are 8-bit wide.

Interfaces

Multibus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Request — All signals TTL compatible

Timer — All signals TTL compatible

Serial I/O — RS232C compatible, data set configuration

BLX — All signals TTL compatible

System Clock (8086 CPU) 4.9152 MHz ± 0.1%

Auxiliary Power

An Auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power down sequences.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min.	Max.	Min.	Max.
Real-time interrupt	1.63 μs	427.1 ms	3.26 s	466.50 min.
Programmable one-shot	1.63 μs	427.1 ms	3.26 s	466.50 min.
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-wave rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software triggered strobe	1.63 μs	427.1 ms	3.26 s	466.50 min.
Hardware triggered strobe	1.63 μs	427.1 ms	3.26 s	466.50 min.
Event Counter	—	2.46 MHz	—	—

Electrical Characteristics: DC Power Requirements

Configuration	Current Requirements			
	V_{CC} = +5V ±5% (max.)	V_{DD} = +12V ±5% (max.)	V_{BB} = −5V ±5% (max.)	V_{AA} = −12V ±5% (max.)
Without EPROM[1]	5.2 A	350 mA	3.2 mA	40 mA
RAM only[2]	10 mA	560 mA	—	40 mA
With 4 K EPROM[3] (using 2758)	5.5 A	350 mA	—	40 mA
With 8 K EPROM[3] (using 2316E)	6.1 A	350 mA	—	40 mA
With 8 K EPROM[3] (using 2716)	5.5 A	350 mA	—	40 mA
With 16 K ROM[3] (using 2732 or 2332A)	5.4 A	350 mA	—	40 mA
With 32 K PROM/ROM[3] (using 2764 or 2364)	6.1 A	350 mA	—	40 mA

Note 1: Does not include power for optional ROM/EPROM. I/O drivers, and I/O terminators.

Note 2: RAM chips powered via auxiliary power bus.

Note 3: Includes power required for four ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Line Drivers and Terminators

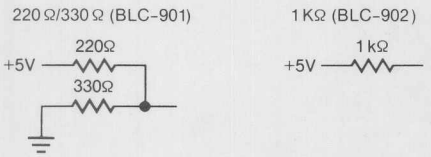
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the BLC-86/12B board.

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note: I = inverting; NI = Non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 K terminators.

I/O Terminators — 220 Ω/330 Ω divider or 1 Ω pull-up



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32

Connectors

Interface	Pine (Qty.)	Centers (In.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12 SAE FUPH7212-86 MTNE
Parallel I/O	50	0.1	3M 3415-000
Serial I/O	26	0.1	3M 3462-000

Physical

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.57 in. (1.45 cm)
Weight — 17.5 oz. (496 grams ± 5%)

Environmental

Operating Temperature — 0°C to 55°C

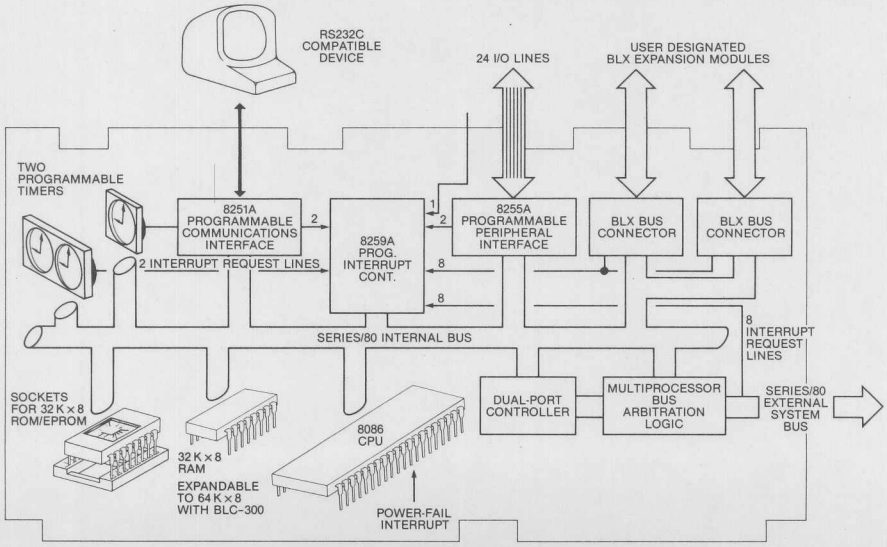
Relative Humidity — 0% to 90% non-condensing

Ordering Information

BLC-86/12B	16-bit board level computer with 32 KB of RAM, sockets for 32 KB ROM/EPROM, 24 parallel I/O lines, RS232C serial port, 2 programmable counters/timers, and 9 levels of vectored interrupts.
BLC-8957	BLC-86/12B Monitor

Documentation

420306302-001	BLC-86/12B Board Level Computer Hardware Reference Manual
420306471-001	BLC-8957 User's Manual

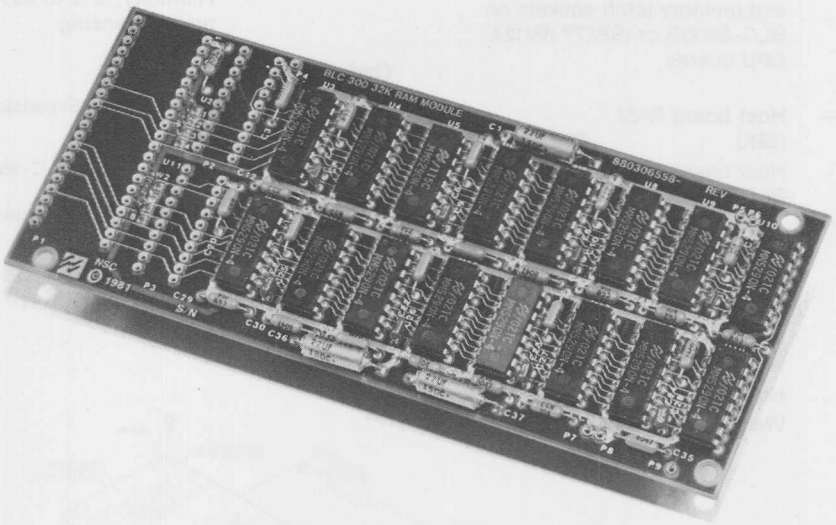


BLC-86/12B Block Diagram

Section 2
Expansion Module Boards

National Semiconductor

BLC-300
32KByte RAM Expansion Module



- **Plugs Directly Into BLC-86/12B or iSBC™ 86/12A Microcomputer**
- **32K Byte Dual Port Dynamic RAM**
- **Accessible by On-Board CPU and Any Other Bus Master**
- **On-Board Installation Reduces MULTIBUS™ Traffic and Increases Access Speed**
- **Minimal Incremental Power Requirements**
- **Address-Assignable Within 1M Byte Memory Space**
- **Plug Replacement for iSBC-300**

Product Overview

The BLC-300 32K Byte RAM Expansion Module is a fast, easy to use, low-cost means of doubling the on-board RAM capacity of the National Semiconductor BLC-86/12B or Intel iSBC 86/12A board level computers from 32K to 64K bytes. Because it plugs directly into device sockets on the host board, it requires no other electrical connections, and is firmly and reliably secured by supplied nylon mounting hardware. When the BLC-300 and host board are installed in the top slot of the BLC-604/614 Card Cage, the combined unit requires only one slot's space. The on-board nature of the BLC-300 memory expansion eliminates the need for additional accessing of the MULTIBUS system bus. Incremental power dissipation of the BLC-300 is only 305mW.

Functional Description

The BLC-300 contains sixteen 16K memory devices which double the on-board RAM capacity of the BLC-86/12B board level computer from 32K to 64K bytes. Three sockets on the BLC-300 are filled with the memory controller and memory latch devices from the BLC-86/12B board. The BLC-300 then plugs directly into the vacant sockets on the BLC-86/12B, completing all electrical connections for both power and board logic in one step. The BLC-300 is then firmly secured at three points with supplied nylon hardware to ensure mechanical stability of the assembled unit.

After the BLC-300 has been secured to the BLC-86/12B, the only adjustment needed on the BLC-86/12B is the changing of two jumper wires.

iSBC and MULTIBUS are trademarks of Intel Corp.

Specifications

Word Size 8 or 16 bits (16-bit data path)

Memory Size 32,768 bytes

Access Time Read: 1.0μs
Write: 1.2μs

Interface Plugs directly into RAM controller and memory latch sockets on BLC-86/12B or iSBC™ 86/12A CPU boards

Addressing
CPU access— Host board RAM (32K) 00000-07FFFH
Host board plus BLC-300 (64K) 00000-0FFFFH

MULTIBUS™ access— Assignable on any 8KByte boundary within any 128KByte boundary in 1MByte system

Physical Length: 5.75 in. (14.60 cm.)
Width: 2.35 in. (5.97 cm.)
Height: 0.50 in. (1.27 cm.)
Weight: 13 oz.(368.55 gm.)

Electrical +5V±5% 1mA
+12V±5% 24mA
−5V±5% 1mA

Environmental Temperature: 0°C to 55°C (32°F to 131°F)
Humidity: 0% to 90% noncondensing

Order Information

BLC-300 32KByte RAM Expansion Module

Documentation

All documentation is contained in BLC-86/12BM (420306302-001)
BLC-86/12B Board Level Computer Hardware Reference Manual

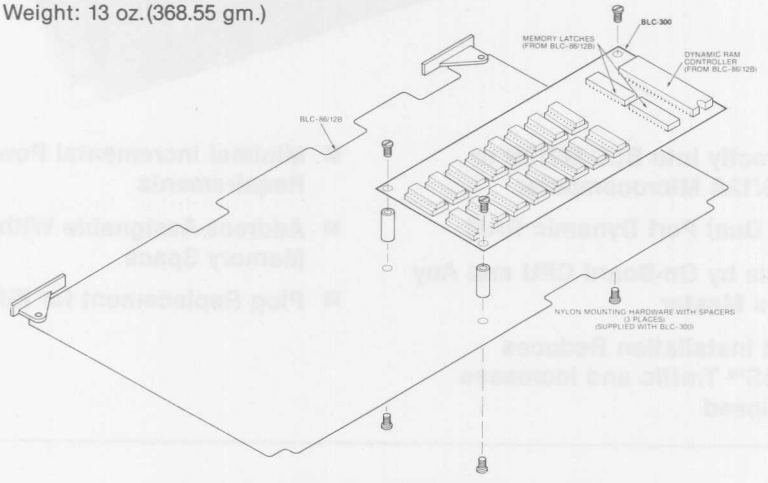
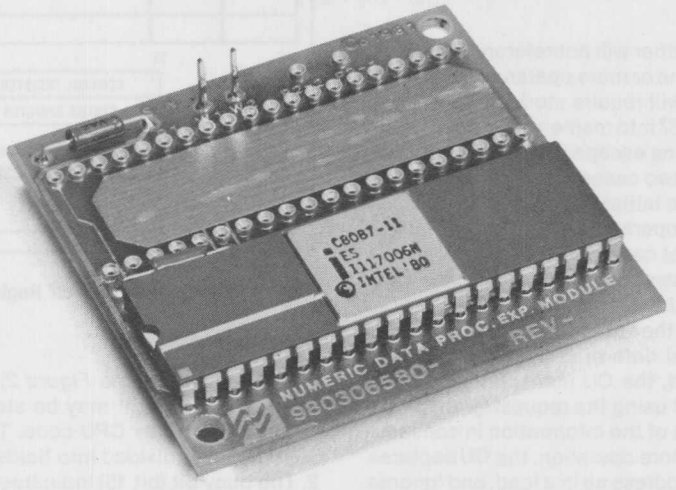


Figure 1. Installation of BLC-300 on BLC-86/12B.

National Semiconductor

BLC-337
Numeric Data Processor Expansion Module



- **Fast fixed and floating point functions for BLC-86/12B and BLC-86/05**
- **Contains the powerful 8087 numeric data processor**
- **Supports single and double precision integer, floating point and others, for a total of seven data types**
- **Plug replacement for Intel SBC-337**
- **Magnifies host CPU instruction set with arithmetic, logarithmic, transcendental, and trigonometric instructions**
- **Proposed IEEE floating point standard is used for high accuracy**
- **Easy to install, plugs into CPU socket on host board**

Product Overview

The BLC-337 is a member of National's growing line of Series/80 Board Level Expansion Modules. High performance numerics support for 8086-based CPU boards such as the BLC-86/12B single board computer user is available for simulation, instrument automation, graphics, signal processing, and business systems. Expanding the instruction set with greater than 60 numeric instructions supporting six data types is provided by coprocessor interface between the 8087 and the CPU. To install the BLC-337, one simply removes the host CPU chip from its socket, plugs the BLC-337 into the host board's CPU socket, and reinstalls the CPU chip into the socket provided on the BLC-337.

Functional Description

The Numeric Data Processor (NDP) is internally divided into two processing elements: the control unit (CU) and the numeric execution unit (NEU), which provides for concurrent operation of the two units. The NEU executes all numeric instructions, while the CU receives and decodes instructions, reads and writes memory operands and executes processor control instructions.

Control Unit

The CU keeps the 8087 operating in synchronization with its host CPU. 8087 instructions are intermixed with CPU instructions in a single instruction stream. The CPU fetches all instructions from memory; by monitoring the status signals emitted by the CPU, the NDP control unit determines when an 8086 instruc-

tion is being fetched. The CU taps the bus in parallel with the CPU and obtains that portion of the data stream.

After decoding the instruction, the host executes all opcodes but ESCAPE (ESC), while the 8087 executes only the ESCAPE class instructions. (The first five bits of all ESCAPE instructions are identical). The CPU does provide addressing for ESC instructions, however.

An 8087 instruction either will not reference memory, will require loading one or more operands from memory into the 8087, or will require storing one or more operands from the 8087 into memory. In the first case, a nonmemory reference escape is used to start 8087 operation. In the last two cases, the CU makes use of a "dummy read" cycle initiated by the CPU, in which a CPU calculates the operand address and initiates a bus cycle, but does not capture the data. Instead, the CPU captures and saves the address which the CPU places on the bus. If the instruction is a load, the CU additionally captures the data word when it becomes available on the local data bus. If data required is longer than one word, the CU immediately obtains the bus from the CPU using the request/grant protocol and reads the rest of the information in consecutive bus cycles. In a store operation, the CU captures and saves the store address as in a load, and ignores the data word that follows in the "dummy read" cycle. When the 8087 is ready to perform the store, the CU obtains the bus from the CPU and writes the operand starting at the specified address.

Numeric Execution Unit

The NEU executes all instructions that involve the register stack; these include arithmetic, logical, transcendental, constant and data transfer instructions. The data path in the NEU is 80 bits wide (64 fraction bits, 15 exponent bits and a sign bit) which allows internal operand transfers to be performed at very high speeds.

When the NEU begins executing an instruction, it activates the 8087 BUSY signal. This signal is used in conjunction with the CPU WAIT instruction to resynchronize both processors when the NEU has completed its current instruction.

Register Set

The 8087 register set is shown in *Figure 1*. Each of the eight data registers in the 8087's register stack is 80 bits wide and is divided into "fields" corresponding to the NDP's temporary real data type.

The register set may be addressed as a push down stack, through a top of stack pointer or any register may be addressed explicitly relative to the top of stack.

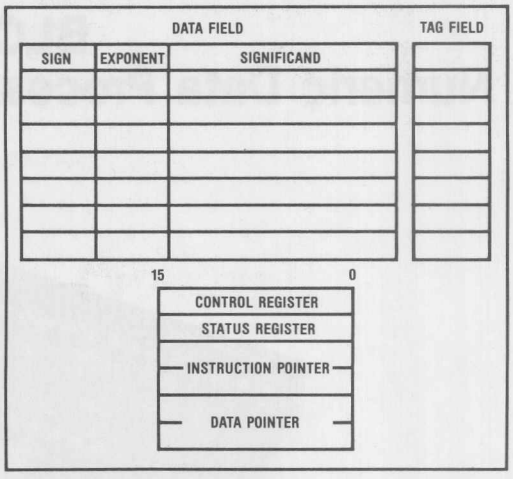


Figure 1. 8087 Register Set

Status Word

The status word (see *Figure 2*) reflects the overall state of the 8087; it may be stored in memory and then inspected by CPU code. The status word is a 16-bit register divided into fields as shown in *Figure 2*. The busy bit (bit 15) indicates whether the NEU is executing an instruction (B = 1) or is idle (B = 0). Several instructions which store and manipulate the status word are executed exclusively by the CU, and these do not set the busy bit themselves.

The four numeric condition code bits (C_0–C_3) are similar to the flags in a CPU: various instructions update these bits to reflect the outcome of NDP operations.

Bits 14–12 of the status word point to the 8087 register that is the current top-of-stack (TOP).

Bit 7 is the interrupt request bit. This bit is set if any unmasked exception bit is set, and cleared otherwise.

Bits 5–0 are set to indicate that the NEU has detected an exception while executing an instruction.

Tag Word

The tag word marks the content of each register as shown in *Figure 3*. The principal function of the tag word is to optimize the NDP's performance. The tag word can be used, however, to interpret the contents of 8087 registers.

Instruction and Data Pointers

The instruction and data pointers (see *Figure 4*) are provided for user-written error handlers. Whenever the 8087 executes an NEU instruction, the CU saves the instruction address, the operand address (if present) and the instruction opcode. The 8087 can then store this data in memory.

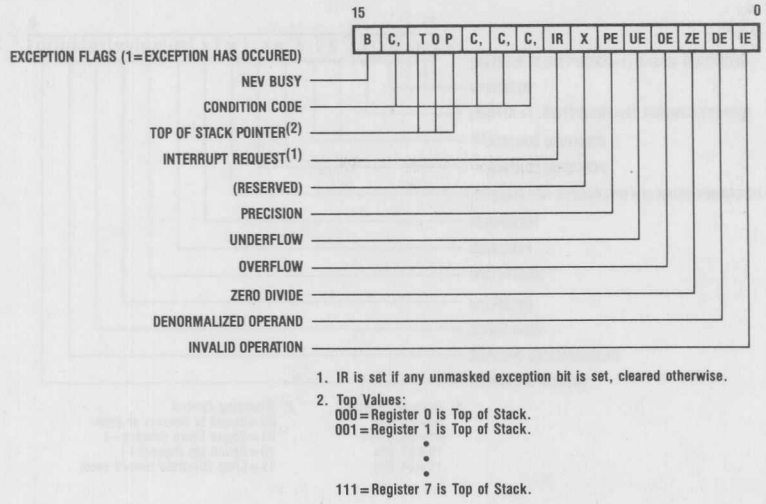


Figure 2. 8087 Status Word

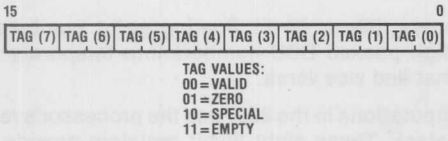


Figure 3. 8087 Tag Word

INSTRUCTION POINTER (15-0)		
INSTRUCTION POINTER (19-16)	0	INSTRUCTION OPCODE (10-0)
DATA POINTER (15-0)		
DATA POINTER (19-16)		0

Figure 4. 8087 Instruction and Data Pointers

Control Word

The NDP provides several processing options which are selected by loading a word from memory into the control word. *Figure 5* shows the format and encoding of the fields in the control word.

Exception Handling

The 8087 detects six different exception conditions that can occur during instruction execution. Any or all exceptions will cause an interrupt if unmasked and interrupts are enabled.

If interrupts are disabled, the 8087 will simply suspend execution until the host clears the exception. If a specific exception class is masked and that exception occurs, however, the 8087 will post the exception in the status register and perform an on-chip default exception handling procedure, thereby allowing processing to continue. The exceptions which the 8087 detects are as follows:

1. INVALID OPERATION: Stack overflow, stack underflow, indeterminate form (0/0, —, etc.) or the use of a Non-Number (NAN) as an operand. An exponent value is reserved and any bit pattern with this value in the exponent field is termed a Non-Number and causes this exception. If this exception is masked, the 8087's default response is to generate a specific NAN called INDEFINITE, or to propagate already existing NANs as the calculation result.
2. OVERFLOW: The result is too large in magnitude to fit the specified format. The 8087 will generate the code for infinity if this exception is masked.
3. ZERO DIVISOR: The divisor is zero while the dividend is a noninfinite, nonzero number. Again, the 8087 will generate the code for infinity if this exception is masked.
4. UNDERFLOW: The result is nonzero but too small in magnitude to fit in the specified format. If this exception is masked, the 8087 will denormalize (shift right) the fraction until the exponent is in range. This process is called gradual underflow.
5. DENORMALIZED OPERAND: At least one of the operands or the result is denormalized; it has the smallest exponent but a nonzero significand. Normal processing continues if this exception is masked off.
6. INEXACT RESULT: If the true result is not exactly representable in the specified format, the result is rounded according to the rounding mode, and this flag is set. If this exception is masked, processing will simply continue.

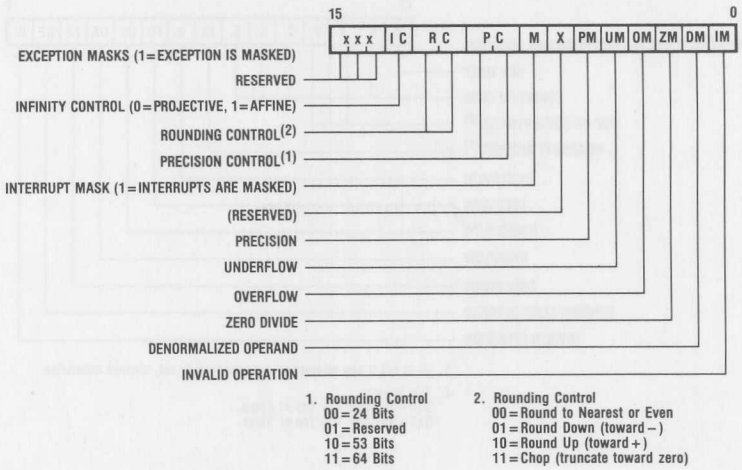


Figure 5. 8087 Control Word

System Configuration

As a coprocessor to an 8086, the 8087 is wired in parallel with the CPU as shown in *Figure 6*. The CPU's status and queue status lines enable the NDP to monitor and decode instructions in synchronization with the CPU and without any CPU overhead. Once started, the 8087 can process in parallel with and independently of the host CPU. For resynchronization, the NDP's BUSY signal informs the CPU that the NDP is executing an instruction and the CPU WAIT instruction tests this signal to ensure that the NDP is ready to execute subsequent instructions. The NDP can interrupt the CPU when it detects an error or exception. The interrupt request line is routed to the CPU through an 8259A Programmable Interrupt Controller. This interrupt request signal is brought down from the BLC-337 module to the 8086-based Board Level Computer through a single pin connector (see *Figure 7*). The signal is then routed to the interrupt matrix for jumper connection to the 8259A Interrupt Controller. By masking off the 8086's "READ" pin from the BLC-337 socket, provisions are made to allow the now vacated pin of the host's CPU socket to be used to bring down the interrupt request signal for connection to the base board and then to the 8259A. Another alternative is to use a wire to establish this connection.

Programming Interface

Table 1 lists the seven data types the 8087 supports and presents the format for each type. Internally, the 8087 holds all numbers in the temporary real format. Load and store instructions automatically convert operands represented in memory as 16-, 32-, or 64-bit integers, 32- or 64-bit floating point numbers or 18-digit packed BCD numbers into temporary real format and vice versa.

Computations in the 8087 use the processor's register stack. These eight 80-bit registers provide the equivalent capacity of 40 16-bit registers. The 8087 register set can be accessed as a stack, with instructions operating on the top stack element, or as a fixed register set, with instructions operating on explicitly designated registers.

Table 3 lists the 8087's instructions by class. Table 2 gives the execution times of some typical numeric instructions and their equivalent time on a 5 MHz 8086.

Coprocessor Interface

The coprocessor interface between the host CPU and the BLC-337 processor provides easy-to-use and high performance math processing. Installation of the BLC-337 processor is simply a matter of removing the host CPU from its socket, installing the BLC-337 processor into the host's CPU socket, and reinstalling the host CPU chip into the socket provided for it on the BLC-337 processor (see *Figure 7*). All synchronization and timing signals are provided via the coprocessor interface with the host CPU. The two processors also share a common address/data bus. (This can be seen in *Figure 6*). The 8087 Numeric Data Processor (NDP) component is capable of recognizing and executing 8087 numeric instructions as they are fetched by the host CPU. This interface allows concurrent processing by the host CPU and the 8087. It also allows 8087 and host CPU instructions to be intermixed in any fashion to provide the maximum overlapped operation and the highest aggregate performance.

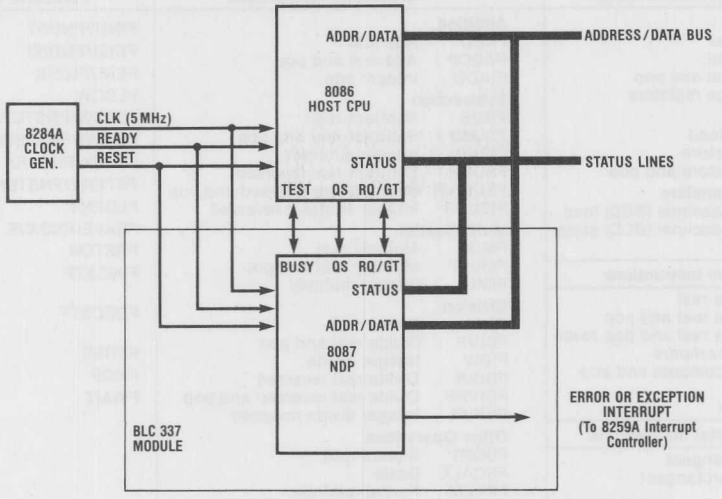


Figure 6. BLC-337 System Configuration

Table 1. 8087 Datatypes

Data Formats	Precision	Range	Most Significant Byte										
			7	07	07	07	07	07	07	07	07	07	0
Word Integer	16 Bits	10^4	I_{15}		I_0								2's Complement
Short Integer	32 Bits	10^9	I_{31}				I_0						2's Complement
Long Integer	64 Bits	10^{19}	I_{63}								I_0		2's Complement
Packed BCD	18 Digits	10^{18}	S	—	D_{17}	D_{16}						D_1	D_0
Short Real	24 Bits	$10^{\pm 36}$	S	E_7	E_0	F_1			F_{23}				F_0 Implicit
Long Real	53 Bits	$10^{\pm 308}$	S	E_{10}	E_0	F_1					F_{52}		F_0 Implicit
Temporary Real	64 Bits	$10^{\pm 4932}$	S	E_{14}			E_0	F_0					F_{63}

Note: Integer: I; Fraction: F; Exponent: E; Sign: S; BCD Digit (4 Bits): D; Packed BCD: $(-1)^8 (D_{17} \ldots D_0)$, Real: $(-1)^8 (2^{E-BIAS}) (F_0 F_1 \ldots)$.
Bias = 127 for Short Real; 1023 for Long Real; 16/383 for Temp Real.

Table 2. Execution Time for Selected 8087 Actual and Emulated Instructions

Floating Point Instruction	Approximate Execution Time (ms)	
	8087 (5MHz Clock)	8086 Emulation
Add/Subtract Magnitude	14/18	1,600
Multiply (single precision)	19	1,600
Multiply (extended precision)	27	2,100
Divide	39	3,200
Compare	9	1,300
Load (double precision)	10	1,700
Store (double precision)	21	1,200
Square Root	36	19,600
Tangent	90	13,000
Exponentiation	100	17,100

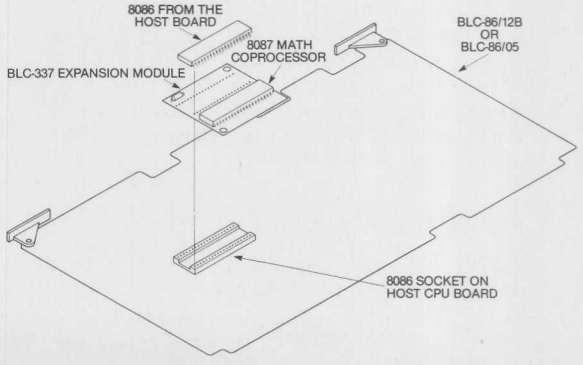


Figure 7. BLC-337 Module Installation

Table 3. 8087 Instruction Set

Data Transfer Instructions		Arithmetic Instructions		Processor Control Instructions	
Real Transfers		**Addition**		FINIT/FNINIT	Initialize processor
FLD	Load real	FADD	Add real	FDISI/FNDISI	Disable Interrupts
FST	Store real	FADDP	Add real and pop	FENI/FNENI	Enable Interrupts
FSTP	Store real and pop	FIADD	Integer add	FLDCW	Load control word
FXCH	Exchange registers	**Subtraction**		FSTCW/FNSTCW	Store control word
Integer Transfers		FSUB	Subtract real	FSTSW/FNSTSW	Store status word
FILD	Integer load	FSUBP	Subtract real and pop	FCLEX/FNCLEX	Clear exceptions
FIST	Integer store	FISUB	Integer subtract	FSTENV/FNSTENV	Store environment
FISTP	Integer store and pop	FSUBR	Subtract real reversed	FLDENV	Load environment
Packed Decimal Transfers		FSUBRP	Subtract real reversed and pop	FSAVE/FNSAVE	Save state
FBLD	Packed decimal (BCD) load	FISUBR	Integer subtract reversed	FRSTOR	Restore state
FBSTP	Packed decimal (BCD) store and pop	**Multiplication**		FINCSTP	Increment stack pointer
Comparison Instructions		FMUL	Multiply real	FDECSTP	Decrement stack pointer
FCOM	Compare real	FMULP	Multiply real and pop	FFREE	Free register
FCOMP	Compare real and pop	FIMUL	Integer multiply	FNOP	No operation
FCOMPP	Compare real and pop twice	**Division**		FWAIT	CPU wait
FICOM	Integer compare	FDIV	Divide real		
FICOMP	Integer compare and pop	FDIVP	Divide real and pop		
FTST	Test	FIDIV	Integer divide		
FXAM	Examine	FDIVR	Divide real reversed		
Transcendental Instructions		FDIVRP	Divide real reversed and pop		
FPTAN	Partial tangent	FIDIVR	Integer divide reversed		
FPATAN	Partial arctangent	**Other Operations**			
F2XM1	2^x-1	FSQRT	Square root		
FYL2X	$Y \cdot \log_2 X$	FSCALE	Scale		
FYL2XP1	$Y \cdot \log_2(X+1)$	FPREM	Partial reminder		
		FRNDINT	Round to integer		
		FXTRACT	Extract exponent and significand		
		FABS	Absolute value		
		FCHS	Change sign		

Specifications

Physical

Width: 5.33cm (2.100″)

Length: 5.08cm (2.000″)

Height: 1.82cm (0.718″)
BLC-337 board + host board

Weight: 17.33 grams (0.576oz.)

Electrical

DC Power Requirements (8087 only)

$V_{CC} = 5V \pm 5\%$

$I_{CC} = 475mA$ max.

Environmental

Operating Temperature — 0°C to 55°C

Free air moving across base board and BLC-337 module

Relative Humidity — Up to 90% noncondensing

Order Information

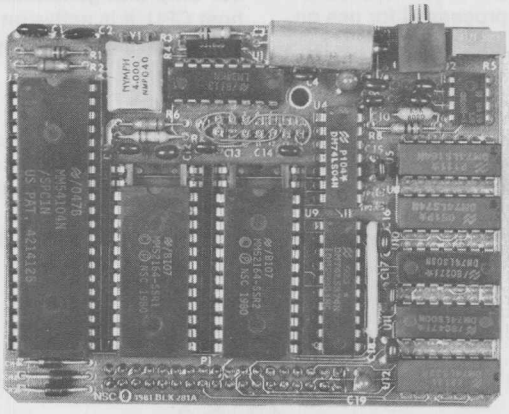
BLC-337	Numeric Data Processor Expansion Module

Documentation

BLC-337M	BLC-337 Numeric Data Processor Expansion Module Hardware Reference Manual (420306580-001)

National Semiconductor

BLX-281
Speech Synthesis Expansion Module



- **BLX bus-compatible I/O expansion**
- **Speech synthesis based on DIGITALKER™**
- **Large vocabulary adequate for most applications**
- **On-board filter and half-watt amplifier**
- **Simple operation for user**
  - I/O write with word/sound address
  - Interrupt asserted when complete
- **BLX bus on-board expansion elimates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-281 Speech Synthesis Expansion Module is a member of the new line of BLX bus-compatible expansion module products from National Semiconductor Corporation. The BLX-281 plugs directly into any BLX bus-compatible host board offering low cost incremental on-board expansion. As a result, any BLX bus-compatible host board may be given the ability to "speak". By merely adding a speaker to a system containing the BLX-281, many users can do away with CRTs, printers, rows of LEDs, or similar communications devices. This lowers the cost of most systems, and has the added benefit of removing messages which are potentially ambiguous and hard-to-understand for untrained users. The BLX-281 contains 144 words, sounds, tones, and durations of silence, each of which has a unique address. A table of addresses (desired words/sounds) is built, and passed to the BLX-281. An on-board filter and amplifier provide the actual speech signal to a standard miniature phone jack. The BLX module is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance, and frees Multibus system traffic for other system resources. Incremental power dissipation is minimal, requiring only 3.7 watts.

DIGITALKER is a trademark of National Semiconductor Corp.

Functional Description

The BLX-281 Speech Synthesis Expansion Module uses the MM54104 Speech Processor Chip from National Semiconductor Corporation. The digitized and compressed speech data are contained in an MM52164 Maxi-ROM. The system software communicates with the BLX-281 across the BLX bus using I/O read/write commands.

Vocabulary

The standard vocabulary set offered on the BLX-281 is shown in Table I, along with the assigned addresses for each item. By combining the appropriate words, sounds, tones, and silence durations, speech can be generated to satisfy many applications.

Words required, but not found in the table, can frequently be built. Examples of this are: combine "RE" with "SET" for "RESET", or combine "DEGREE" with "SS" for "DEGREES".

In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. This is provided for in the BLX-281 (see Table I). A suggestion for improved phrase quality is to insert 80 milliseconds of silence prior

Multibus is a trademark of Intel Corp.

to words beginning with the letters K, T, P, B, D, and G, and to add 40 milliseconds of silence after words ending in those same letters.

The "voice" output of the BLX-281 is a highly intelligible, male voice. If another voice is required, or the application is non-English, or involves unusual terminology, any voice can be processed for use on the BLX-281 by the factory.

Host Interface

The BLX bus-compatible host board merely passes the address of the desired word/sound to the BLX-281 Speech Synthesis Expansion Module via an I/O write. When the operation is complete, an interrupt is generated. This informs the host of the end of the speech sequence, and allows for cascading of addresses for true, human-quality sentences.

Interrupt Requests

There is one interrupt line from the Speech Processor Chip that generates an interrupt request to the host CPU. It is active on completion of each speech sequence. It is cleared by an I/O read to the BLX-281.

Installation

The BLX-281 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 1 and 2).

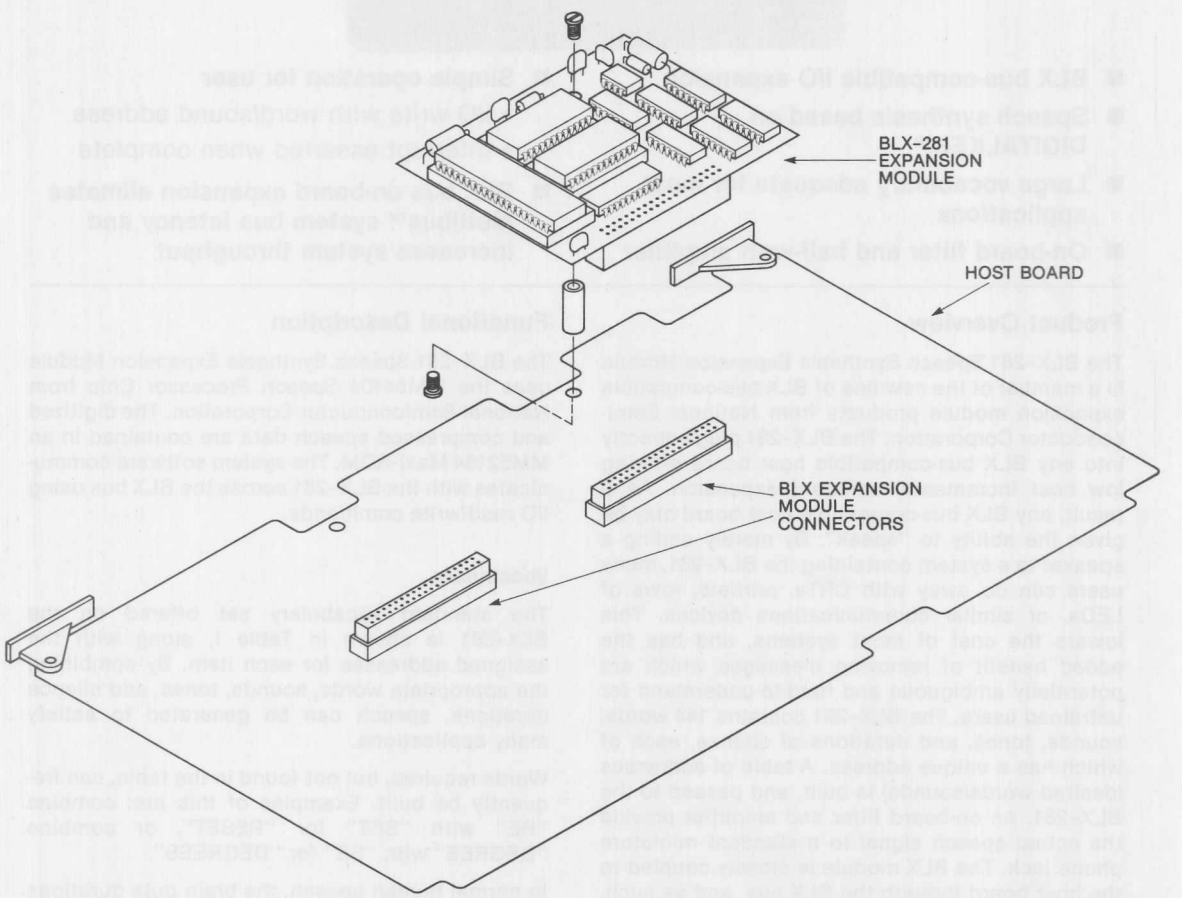


Figure 1. Installation of the BLX-281 Module on a Host Board

Table I. Master Word List

Word	8-Bit Binary Address Bit 7 Bit 0	Word	8-Bit Binary Address Bit 7 Bit 0	Word	8-Bit Binary Address Bit 7 Bit 0
THIS IS DIGITALKER	00000000	Q	00110000	IS	01100000
ONE	00000001	R	00110001	IT	01100001
TWO	00000010	S	00110010	KILO	01100010
THREE	00000011	T	00110011	LEFT	01100011
FOUR	00000100	U	00110100	LESS	01100100
FIVE	00000101	V	00110101	LESSER	01100101
SIX	00000110	W	00110110	LIMIT	01100110
SEVEN	00000111	X	00110111	LOW	01100111
EIGHT	00001000	Y	00111000	LOWER	01101000
NINE	00001001	Z	00111001	MARK	01101001
TEN	00001010	AGAIN	00111010	METER	01101010
ELEVEN	00001011	AMPERE	00111011	MILE	01101011
TWELVE	00001100	AND	00111100	MILLI	01101100
THIRTEEN	00001101	AT	00111101	MINUS	01101101
FOURTEEN	00001110	CANCEL	00111110	MINUTE	01101110
FIFTEEN	00001111	CASE	00111111	NEAR	01101111
SIXTEEN	00010000	CENT	01000000	NUMBER	01110000
SEVENTEEN	00010001	400 Hz TONE	01000001	OF	01110001
EIGHTEEN	00010010	80 Hz TONE	01000010	OFF	01110010
NINETEEN	00010011	20 ms SILENCE	01000011	ON	01110011
TWENTY	00010100	40 ms SILENCE	01000100	OUT	01110100
THIRTY	00010101	80 ms SILENCE	01000101	OVER	01110101
FORTY	00010110	160 ms SILENCE	01000110	PARENTHESIS	01110110
FIFTY	00010111	320 ms SILENCE	01000111	PERCENT	01110111
SIXTY	00011000	CENTI	01001000	PLEASE	01111000
SEVENTY	00011001	CHECK	01001001	PLUS	01111001
EIGHTY	00011010	COMMA	01001010	POINT	01111010
NINETY	00011011	CONTROL	01001011	POUND	01111011
HUNDRED	00011100	DANGER	01001100	PULSES	01111100
THOUSAND	00011101	DEGREE	01001101	RATE	01111101
MILLION	00011110	DOLLAR	01001110	RE	01111110
ZERO	00011111	DOWN	01001111	READY	01111111
A	00100000	EQUAL	01010000	RIGHT	10000000
B	00100001	ERROR	01010001	SS	10000001
C	00100010	FEET	01010010	SECOND	10000010
D	00100011	FLOW	01010011	SET	10000011
E	00100100	FUEL	01010100	SPACE	10000100
F	00100101	GALLON	01010101	SPEED	10000101
G	00100110	GO	01010110	STAR	10000110
H	00100111	GRAM	01010111	START	10000111
I	00101000	GREAT	01011000	STOP	10001000
J	00101001	GREATER	01011001	THAN	10001001
K	00101010	HAVE	01011010	THE	10001010
L	00101011	HIGH	01011011	TIME	10001011
M	00101100	HIGHER	01011100	TRY	10001100
N	00101101	HOUR	01011101	UP	10001101
O	00101110	IN	01011110	VOLT	10001110
P	00101111	INCHES	01011111	WEIGHT	10001111

Note: Address $8F_H$ is the last legal address in this word list. Exceeding address $8F_H$ will produce pieces of unintelligible, invalid speech data.

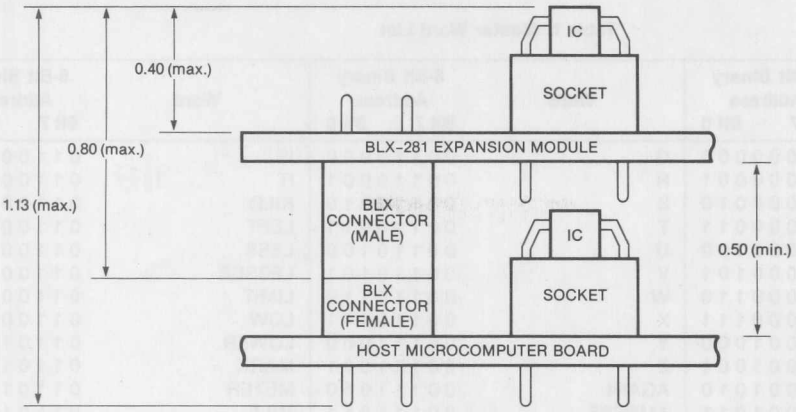


Figure 2. BLX-281 Expansion Module Mounting Clearances (inches)

Specifications

Word Size

Data — 8 bits

I/O Addressing

Function	Type of Operation	BLX Connector Port Address
Data Transfer	Write	X0-XF
Interrupt Clear	Read	X0-XF

Note: The port addresses are determined on the host BLC microcomputer. Refer to the Hardware Reference Manual for your host BLC microcomputer to determine the first digit (X) of the connector port address.

Vocabulary — See Table I

Interrupts — One interrupt request at end of speech sequence

Interfaces — BLX Bus — All signals TTL compatible
Speaker Port — ½W audio signal into 4-8Ω

Speaker Port Connector — Standard miniature phone-jack

Physical
Height: 2.85 in. (7.24 cm)
Width: 3.70 in. (9.40 cm)
Depth
BLX-281 Module
0.80 in. (2.04 cm)
BLX-281 Module + Host Board
1.13 in. (2.86 cm)
Weight: 1.7 oz. (48 gm)

Electrical
+5 VDC ± 5% @ 385 mA
+12 VDC ± 5% @ 150 mA

Environmental
Operating Temperature: 0°C to 55°C
Relative Humidity: 0% to 90%, non-condensing

Ordering Information

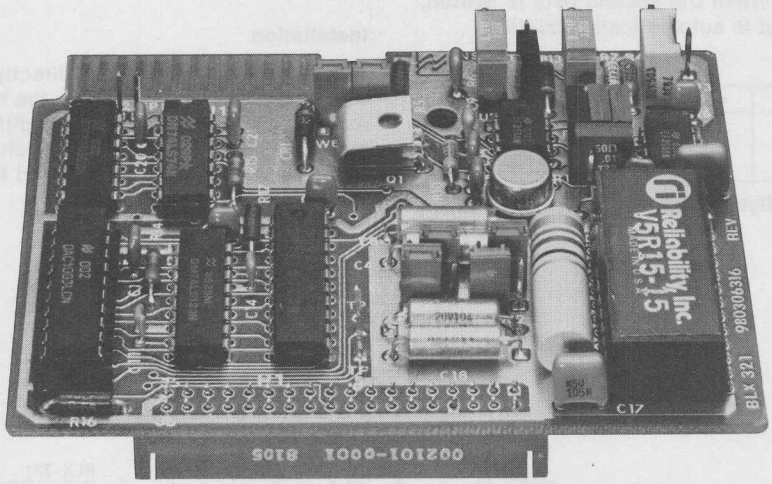
BLX-281	Speech Synthesis Expansion Module

Documentation

420306414-001	BLX-281 Speech Synthesis Expansion Module User's Manual

National Semiconductor

BLX-321
Analog Output Expansion Module



- **BLX bus-compatible I/O expansion**
- **Single channel of digital-to-analog conversion**
- **10-bit resolution with high accuracy**
- **Concurrent voltage and current modes**
- **Single +5V DC power required**
- **BLX bus on-board expansion eliminates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-321 Analog Output Expansion Module is a member of the new line of BLX bus-compatible expansion modules from National Semiconductor Corporation. The BLX-321 plugs directly into any BLX bus-compatible host board offering incremental on-board expansion. The BLX-321 provides a single channel of digital-to-analog conversion. Ten-bit resolution is provided with an accuracy of 0.05% of the desired output plus ½ LSB. Current and voltage modes are simultaneously provided. An on-board DC-to-DC converter provides all required voltages from the $+5V_{DC}$ on the BLX bus. The user can optionally provide his own power if his application requires high voltage compliance into large loads. The BLX board is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance and frees Multibus system traffic for other system resources. In addition, incremental power dissipation is minimal, requiring only 3.5 watts.

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Functional Description

Analog Section

The BLX-321 Analog Output Expansion Module uses a DAC1006 digital-to-analog converter from National Semiconductor Corporation to provide a single analog output channel. The output is a constant current (4 to 20 mA) and a constant voltage (0 to 10 V). The 10-bit resolution offers 0.16 μA steps in the current mode and 10 mV steps in the voltage mode.

The output connector (J1) is a 26-pin edge connector that mates with flat, woven, or round cable. By using different combinations of output pins, the user selects which current or voltage modes are desired (different modes allow for differing burdens). The connection for the optional user-supplied power (for current mode into high loads) is also on J1.

Host Interface

The ten bits of data, representing the desired analog output, are passed to the BLX-321 by I/O write commands, (The first byte contains the most significant two bits.) and are stored for the DAC1006. They need only be rewritten if they need to be changed. The second byte contains the eight least significant bits. When the second byte is written, the analog output is automatically updated.

7	6	5	4	3	2	1	0
X	X	X	X	X	X	Data 9 (MSB)	Data 8

First Byte (Most Significant)

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0 (LSB)

Second Byte (Least Significant)

Installation

The BLX-321 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figure 1 and Figure 2).

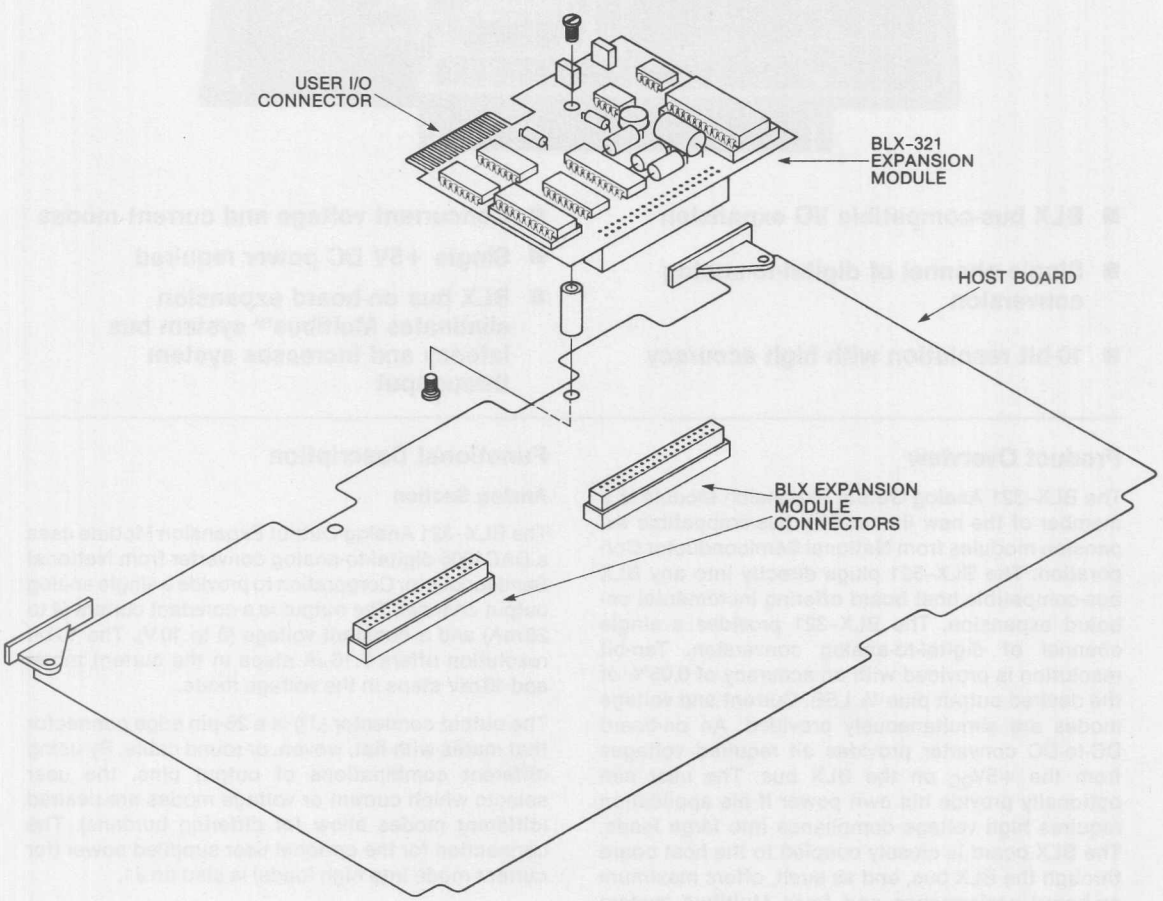


Figure 1. Installation of BLX-321 Module on a Host Board

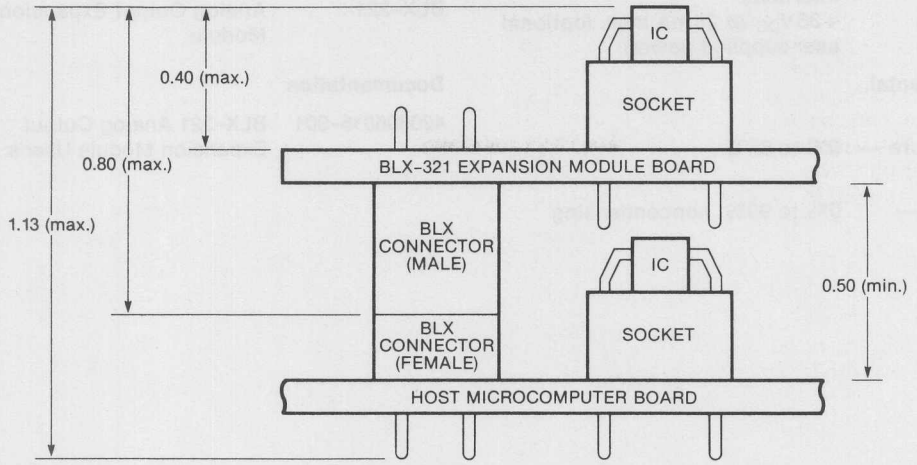


Figure 2. BLX-321 Expansion Module Mounting Clearances (inches)

Specifications

General

Number of Channels — One

Channel Resolution — 10 bits

Slew Rate — Full scale in 1.0 μs

Settling Time — 3.0 μs to ½LSB (half scale step change)

Overall Accuracy — ±[0.05% settling + ½LSB] (15°C to 35°C)

Accuracy Tempco — ±[0.001% setting + 0.002% full scale]/°C

Monotonicity — Guaranteed over operating temperature range

Voltage Mode Output Characteristics

Output Range — 0 to +10 V

Output Current — 5 mA@10 V_{DC}

Output Steps — 10 mV

Current Mode Output Characteristics

Output Range — 4 to 20 mA current loop, unipolar

Load Impedance — 0 Ω to 500 Ω (with 15 V_{DC} on-board voltage reference)
0 Ω to 1.5 KΩ (with 35 V_{DC} user-supplied voltage reference)

I/O Addressing

Function	BLX-321 Address
MS Byte Write	X0,X2,X4,X6, X8,XA,XC,XE
LS Byte Write	X1,X3,X5,X7, X9,XB,XD,XF

Note: The first digit of each port I/O address is listed as "X" since it will change dependent upon the type of host BLC microcomputer used. Refer to the Hardware Reference Manual for your host microcomputer to determine the first digit of the port address.

Access Time

50 ns max.

Note: Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Interfaces

BLX-Bus: All signals TTL compatible
Analog Output: 0-10 V, 4-20 mA

Analog I/O Connector

One 26-pin, double-sided, card edge connector on 0.1" centers

Recommended mating connectors:
3M 3462-0001
AMP 1-583715-1

Physical

Height 2.85 in. (7.25 cm)
Width 3.70 in. (9.40 cm)
Depth
BLX-321 Module
Depth
BLX-321 + Host Board
Depth
Weight 2.2 oz. (62.37 gm.)

Electrical	+5 V_{DC} @ 0.7 A max. (BLX interface) +35 V_{DC} @ 23 mA max. (optional user-supplied power)
Environmental	
Operating Temperature —	0°C to 55°C
Relative Humidity —	0% to 90%, noncondensing

Ordering Information

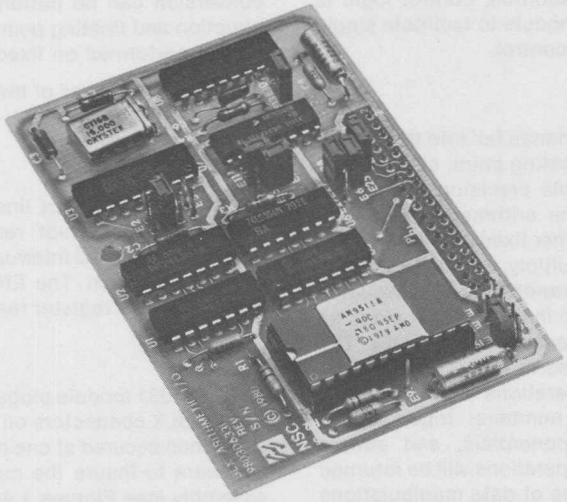
BLX-321	Analog Output Expansion Module

Documentation

420306316-001	BLX-321 Analog Output Expansion Module User's Manual

National Semiconductor

BLX-331
Fixed/Floating Point Math Expansion Module



- **BLX bus compatible high speed fixed/floating point math expansion**
- **4 MHz operation**
- **Fixed point single and double precision (16/32-bit)**
- **Floating point double precision (32-bit)**
- **Binary data formats**
- **Add, subtract, multiply, and divide**
- **Trigonometric and inverse trigonometric functions**
- **Square root, log, and exponential functions**
- **Float to fixed and fixed to float conversions**
- **End of operation interrupt**
- **Software reset control**
- **Low power requirements**
- **BLX bus on-board expansion eliminates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-331 Fixed/Floating Point Math Expansion Module is a member of the new line of BLX bus-compatible expansion module products from National Semiconductor Corporation. The BLX-331 plugs directly into any BLX bus-compatible host board offering low cost incremental on-board expansion. As a result, any BLX bus-compatible host board may be expanded to perform high speed math computations, affording up to a 40 times improvement in speed compared to software math. The BLX-331 module performs single/double (16/32-bit) precision fixed point plus double (32-bit) precision floating point arithmetic operations. In addition, the module performs transcendental, data manipulation, and fixed-to-float/float-to-fixed point conversion operations. The command operations run entirely independent of the host board permitting efficient concurrent processing. The BLX module is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance and frees Multibus system traffic for other system resources. Incremental power dissipation is minimal, requiring only 2.73 watts.

Functional Description

The BLX-331 module uses the 8231 Arithmetic Processing Unit (APU) to accomplish high speed (4 MHz) math operation. The system software may communicate with the BLX-331 module across the BLX bus using I/O read/write commands. All transfers, including operand, result, status, and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an

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internal stack and commands are issued to perform operations on the data. Results are then available from the stack. A status byte may be read to monitor execution completion and the nature of the result (zero, sign, or errors). In addition, control logic is included on the BLX-331 module to facilitate single instruction software reset control.

Command Functions

The BLX-331 module commands fall into three categories: double precision floating point, single precision fixed point, and double precision fixed point (see Table I). There are four arithmetic operations that can be performed in either fixed or floating point numbers: add, subtract, multiply, and divide. These operations require two operands. The 8231 assumes these operands are located in the internal stack as Top-of-Stack (TOS) and Next-on-Stack (NOS). The result will always be returned to TOS. There are four types of transcendental operations that can be performed in floating point numbers: trigonometric functions, logarithms, exponentials, and square roots. The results of these operations will be returned to TOS. There are four types of data manipulations operations that can be performed in either fixed or floating point numbers: sign change of TOS, exchange of TOS and NOS, and copying or popping operands onto or off of TOS. Fixed to floating point conversion can be performed on floating point instruction and floating point to fixed point conversion can be performed on fixed point instructions.

The execution times of the commands are shown in Table II.

Interrupt Requests

There is one interrupt line from the APU that may generate an interrupt request to the host: END (MINTR1). The END interrupt line is active upon command completion. The END signal is cleared by a reset or status register read.

Installation

The BLX-331 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 1 and 2).

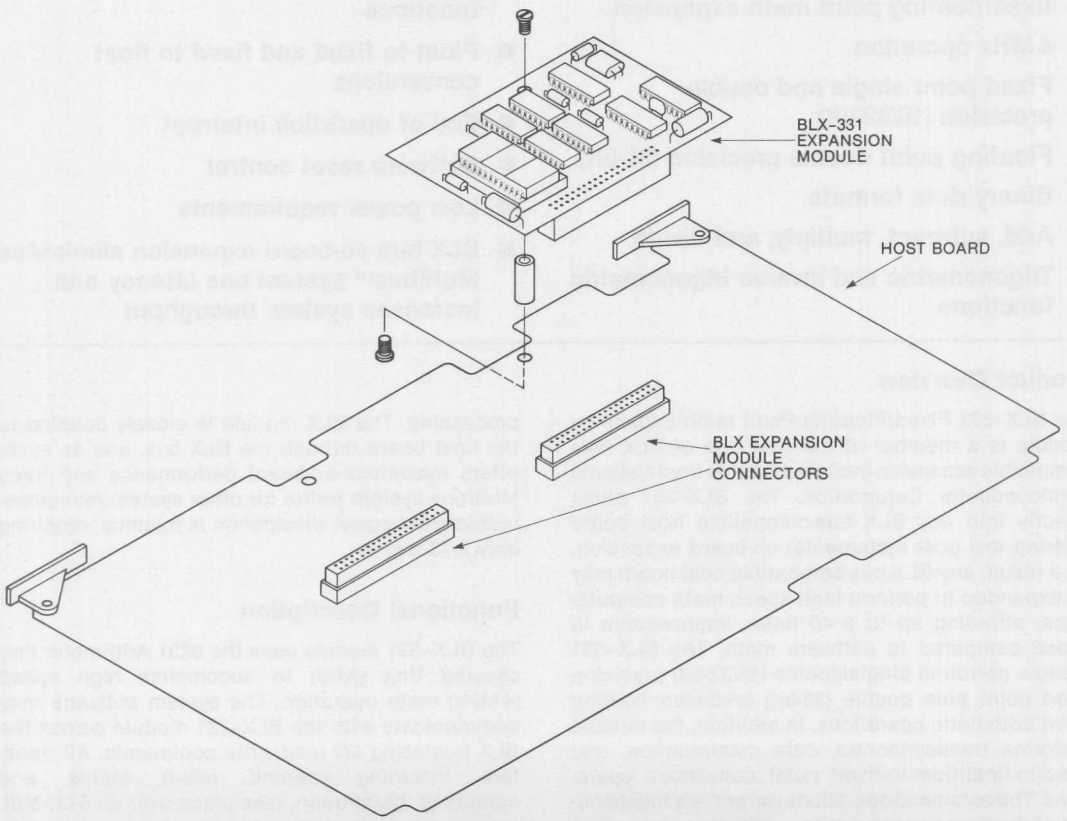


Figure 1. Installation of the BLX-331 Module on a Host Board

Table I. Command Summary

Instruction	Description	Hex Code	Stack Contents After Execution[1] A B C D	Status Flags Affected[3]
Double Precision Floating Point Instructions (32-Bit)				
ACOS	Inverse Cosine of A	0 6	R U U U	S, Z, E
ASIN	Inverse Sine of A	0 5	R U U U	S, Z, E
ATAN	Inverse Tangent of A	0 7	R B U U	S, Z
CHSF	Sign Change of A	1 5	R B C D	S, Z
COS	Cosine of A (radians)	0 3	R B U U	S, Z
EXP	e^A Function	0 A	R B U U	S, Z, E
FADD	Add A and B	1 0	R C D U	S, Z, E
FDIV	Divide B by A	1 3	R C D U	S, Z, E
FLTD	32-Bit Fixed-to-Floating Point Conversion	1 C	R B C U	S, Z
FLTS	16-Bit-Fixed-to-Floating Point Conversion	1 D	R B C U	S, Z
FMUL	Multiply A and B	1 2	R C D U	S, Z, E
FSUB	Subtract A from B	1 1	R C D U	S, Z, E
LOG	Common Logarithm (base 10) of A	0 8	R B U U	S, Z, E
LN	Natural Logarithm of A	0 9	R B U U	S, Z, E
POPF	Stack Pop	1 8	B C D A	S, Z
PTOF	Stack Push	1 7	A A B C	S, Z
PUPI	Push π onto Stack	1 A	R A B C	S, Z
PWR	B^A Power Function	0 B	R C U U	S, Z, E
SIN	Sine of A (radians)	0 2	R B U U	S, Z
SQRT	Square Root of A	0 1	R B C U	S, Z, E
TAN	Tangent of A (radians)	0 4	R B U U	S, Z, E
XCHF	Exchange A and B	1 9	B A C D	S, Z
Double Precision Fixed Point Instructions (32-Bit)				
CHSD	Sign Change of A	3 4	R B C D	S, Z, O
DADD	Add A and B	2 C	R C D A	S, Z, C, E
DDIV	Divide B by A	2 F	R C D U	S, Z, E
DMUL	Multiply A and B (R = lower 32 bits)	2 E	R C D U	S, Z, O
DMUU	Multiply A and B (R = upper 32 bits)	3 6	R C D U	S, Z, O
DSUB	Subtract A from B	2 D	R C D A	S, Z, C, O
FIXD	Floating to Fixed Point Conversion	1 E	R B C U	S, Z, O
POPD	Stack Pop	3 8	B C D A	S, Z
PTOD	Stack Push	3 7	A A B C	S, Z
XCHD	Exchange A and B	3 9	B A C D	S, Z

Table I. Command Summary (continued)

Instruction	Description	Hex Code	Stack Contents After Execution[2] A_U A_L B_U B_L C_U C_L D_U D_L	Status Flags Affected[3]
Single Precision Fixed Point Instructions (12-Bit)				
CHSS	Change Sign of A_U	7 4	R A_L B_U B_L C_U C_L D_U D_L	S, Z, O
FIXS	Floating to Fixed Point Conversion	1 F	R B_U B_L C_U C_L U U U	S, Z, O
POPS	Stack Pop	7 8	A_L B_U B_L C_U C_L D_U D_L A_U	S, Z
PTOS	Stack Push	7 7	A_U A_U A_L B_U B_L C_U C_L D_U	S, Z
SADD	Add A_U and A_L	6 C	R B_U B_L C_U C_L D_U D_L A_U	S, Z, C, E
SDIV	Divide A_L by A_U	6 F	R B_U B_L C_U C_L D_U D_L U	S, Z, E
SMUL	Multiply A_L by A_U (R = lower 16 bits)	6 E	R B_U B_L C_U C_L D_U D_L U	S, Z, E
SMUU	Multiply A_L by A_U (R = upper 16 bits)	7 6	R B_U B_L C_U C_L D_U D_L U	S, Z, E
SSUB	Subtract A_U from A_L	6 D	R B_U B_L C_U C_L D_U D_L A_U	S, Z, C, E
XCHS	Exchange A_U and A_L	7 9	A_L A_U B_U B_L C_U C_L D_U D_L	S, Z
NOP	No Operation	0 0	A_U A_L B_U B_L C_U C_L D_U D_L	

Note 1: The stack initially is composed of four 32-bit numbers (A, B, C, D). A is equivalent to Top-of-Stack (TOS) and B is Next-on-Stack (NOS). Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A, B, C, or D).

Note 2: The stack initially is composed of eight 16-bit numbers (A_U, A_L, B_U, B_L, C_U, C_L, D_U, D_L). A_U is the TOS and A_L is NOS. Upon completion of a command the stack is composed of: the result (R); undefined (U); or the intial contents (A_U, A_L, B_U, B_L, . . .).

Note 3: Nomenclature: Sign (S); Zero (Z); Overflow (O); Carry (C), Error Code Field (E).

Table II. Command Execution Times

Command Mnemonic	μSeconds	Command Mnemonic	μSeconds
SADD	4.25	ASIN	1917
SSUB	7.5	ACOS	1933.5
SMUL	21–23.5	ATAN	1501.5
SMUU	20–24.5	LOG	1118.5–1783
SDIV	21–23.5	LN	1074.5–1739
DADD	5.25	EXP	948.5–1219.5
DSUB	9.5	PWR	2072.5–3008
DMUL	48.5–52.5	NOP	1.0
DMUU	45.5–54.5	CHSS	5.75
DDIV	52	CHSD	6.75
FIXS	23-54	CHSF	4.5
FIXD	25–86.5	PTOS	4.0
FLTS	24.5–46.5	PTOD	5.0
FLTD	24.5–94.5	PTOF	5.0
FADD	13.5–92	POPS	2.5
FSUB	17.5–92.5	POPD	3.0
FMUL	36.5–42	POPF	3.0
FDIV	38.5–46	XCHS	4.5
SORT	200	XCHD	6.5
SIN	1116	XCHF	6.5
COS	1029.5	PUPI	4.0
TAN	1438.5		

Note: Assumes 4 MHz operation.

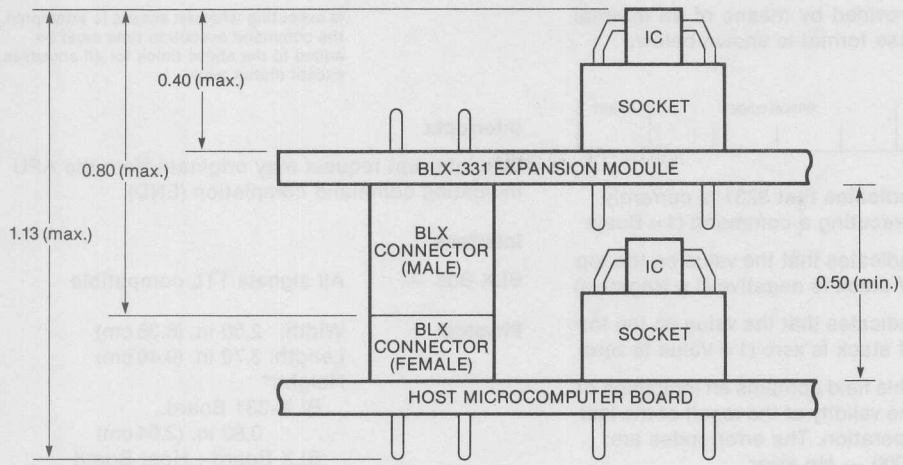


Figure 2. BLX-331 Expansion Module Mounting Clearances (inches)

Specifications

Word Size

Data — 8-bits

On-Board Clock Rate

4.0 MHz ± 0.1%

I/O Addressing

Function	Type of Operation	BLX Connector Port Address
Data Transfer	Read/Write	X0, X2, X4, or X6
Command Transfer	Write	X1, X3, X5, or X7
Status Transfer	Read	X1, X3, X5, or X7
Reset	Write	X8 through XF

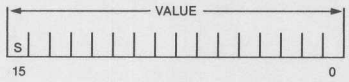
Note: The port addresses are determined on the host BLC microcomputer. Refer to the Hardware Reference Manual for your host BLC microcomputer to determine the first digit (X) of the connector port address.

Arithmetic Functions

See Table I

Data Formats

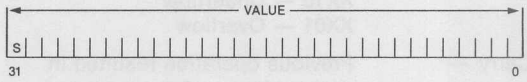
Single Precision Fixed Point (16 Bits)



Bits 15: S = Sign of the operand. Positive values are represented by a sign bit of zero (S = 0). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 (S = 1).

Bits 0-14: Values in the range from −32, 768 to +32, 767.

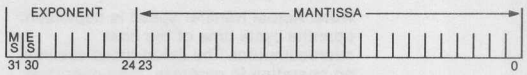
Double Precision Fixed Point (32 bits)



Bit 31: S = Sign of operand. Positive values are represented by a sign of zero (S = 0). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 (S = 1).

Bits 0-30: Values in the range from −2, 147, 483, 648 to +2, 147, 483, 647.

Double Precision Floating Point (32 bits)



Bit 31: MS = Sign of the mantissa. 1 represents negative and 0 represents positive.

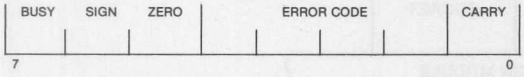
Bits 24-30: ES = The exponent expressed as a two's complement 7-bit value having a range of −64 to +63.

Bits 0-23: The mantissa is expressed as a 24-bit (fractional) value. The 8231 APU requires that floating point data be represented by a fractional mantissa value between 0.5 and 1 multiplied by 2 raised to an appropriate power (exponent). This is expressed as follows:

$$\text{Value} = \text{mantissa} \times 2^{\text{EXPONENT}}$$

Device Status

Device status is provided by means of an internal status register whose format is shown below:



Busy — Indicates that 8231 is currently executing a command (1 = Busy)

Sign — Indicates that the value on the top of stack is negative (1 = Negative)

Zero — Indicates that the value on the top of stack is zero (1 = Value is zero)

Error Code — This field contains an indication of the validity of the result of the last operation. The error codes are:
0000 — No error
1000 — Divide by zero
0100 — Square root or log of negative number
1100 — Argument of inverse sine, cosine, or e^X too large
XX10 — Underflow
XX01 — Overflow

Carry — Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow.)

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

Access Time

Read — 1900 ns (max.)

Write — 1900 ns (max.)

Note: Actual transfer speed is dependent uponthe cycle time of the host microcomputer. The listed times assume no operation in progress. If an operation is executing when an access is attempted, the command execution time must be added to the above times for all accesses except status read.

Interrupts

One interrupt request may originate from the APU indicating command completion (END).

Interface

BLX Bus — All signals TTL compatible

Physical

Width: 2.50 in. (6.35 cm)
Length: 3.70 in. (9.40 cm)
Height:*
BLX-331 Board
0.80 in. (2.04 cm)
BLX Board + Host Board
1.13 in. (2.86 cm)
Weight: 1.79 oz. (51 gm)
*See Figure 2.

Electrical

DC Power Requirements
+5V ± 5% @ 365 mA max.
+12V ± 5% @ 75 mA max.

Environmental

Operating Temperature:
0°C to 55°C
Humidity:
0% to 90%, non-condensing

Ordering Information

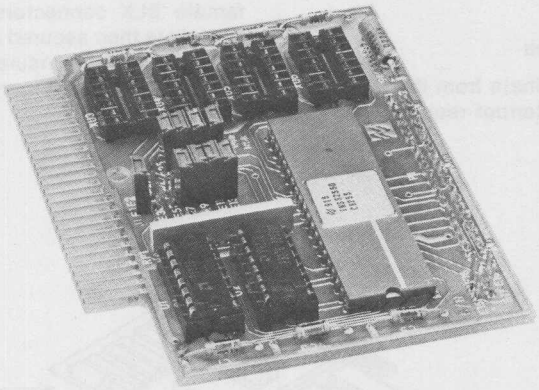
BLX-331 Fixed/Floating Point Math Expansion Module

Documentation

420306331-001 BLX-331 Fixed/Floating Point Math Expansion Module/BLX-332 Floating Point Math Expansion Module User's Manual

National Semiconductor

BLX-350
Parallel I/O Expansion Module



- **BLX bus compatible I/O expansion**
- **24 programmable I/O lines with sockets for interchangeable line drivers and terminators**
- **Three jumper selectable interrupt request sources**
- **Accessed as I/O port locations**
- **Single +5V lower power requirement**
- **BLX bus on-board expansion eliminates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-350 Parallel I/O Expansion Module is a member of the new line of BLX bus compatible expansion modules from National Semiconductor Corporation. The BLX-350 plugs directly into any BLX bus compatible host board offering incremental on-board expansion. The BLX-350 module provides 24 programmable I/O lines with sockets for interchangeable line drivers and terminators. The BLX board is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance and frees Multibus system traffic for other system resources. In addition, incremental power dissipation is minimal, requiring only 1.6 watts (not including optional driver/terminators).

Functional Description

Programmable Interface

The BLX-350 module uses an 8255A-5 Programmable Peripheral Interface (PPI) providing 24 parallel I/O lines. The base-board system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table I. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further

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enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and driver/termination characteristics for each application. In addition, inverting bidirectional bus drivers (8226) are provided on sockets to allow convenient optional replacement to non-inverting drivers (8216). The 24 programmable I/O lines, signal ground, and +5 volt power (jumper configurable) are brought to a 50-pin edge connector that mates with flat, woven, or round cable.

Interrupt Request Generation

Interrupt requests may originate from three jumper selectable sources. Two interrupt requests can be automatically generated by the PPI when a byte of information is ready to be transferred to the base board CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). A third interrupt source may originate directly from the user I/O interface (J1 connector).

Installation

The BLX-350 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figure 1 and Figure 2).

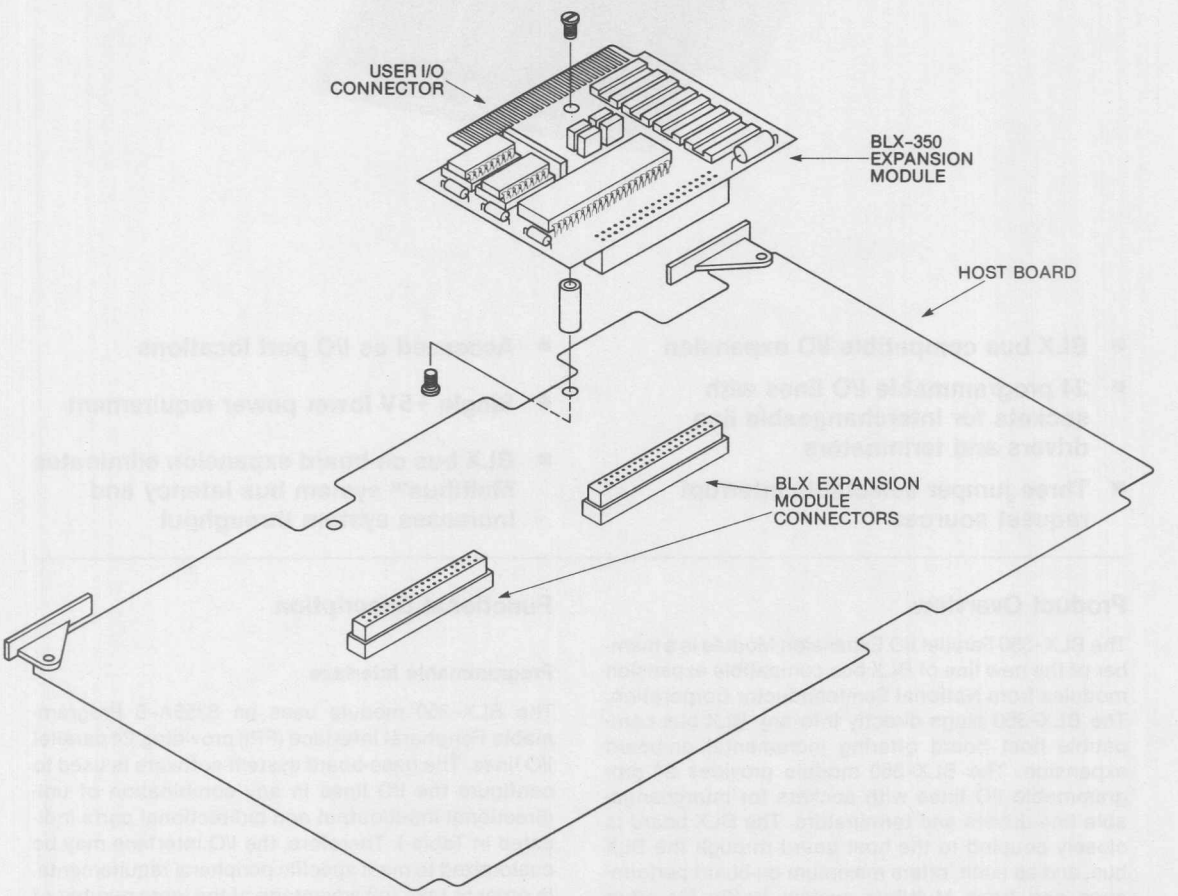


Figure 1. Installation of BLX-350 Module on a Host Board

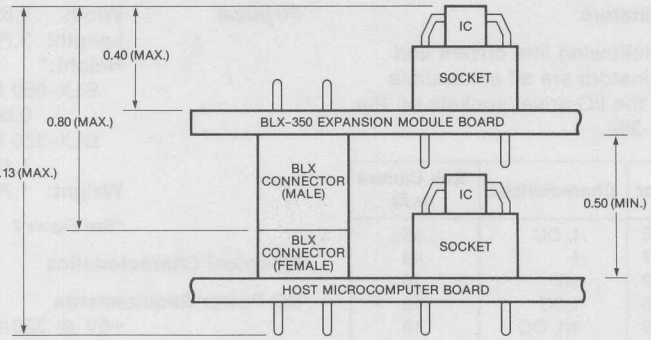


Figure 2. BLX-350 Expansion Module Mounting Clearances (inches)

Table I. Input/Output Port Modes of Operation

Port	Lines (Qty.)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
A	8	X	X	X	X	X	
B	8	X	X	X	X		
C	4	X		X			X[1]
	4	X		X			X[1]

Note 1. Part of port C must be used as a control port when either port A or port B are used as a latched and strobed input or a latched and strobed output port, or port A is used as a bidirectional port.

Specifications

Word Size

Data — 8 Bits

I/O Addressing

8255A-5 Ports	BLX-350 Address
Port A	X0 or X4
Port B	X1 or X5
Port C	X2 or X6
Control	X3 or X7
Reserved	X8 to XF

Note: The first digit of each port I/O address is listed as "X" since it will change dependent upon the type of host BLC microcomputer used. Refer to the Hardware Reference Manual for your host BLC microcomputer to determine the first digit of the port address.

I/O Capacity 24 programmable lines (see Table I)

Access Time Read: 250 ns max.
Write: 300 ns max.

Note: Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Interrupts Interrupt requests may originate from the programmable peripheral interface (2) or the user specified I/O (1).

Interfaces

BLX Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Parallel I/O Connectors All 25 pairs/50 pins on 0.1″ centers

Connector Type	Vendor	Vendor Part No.
Female	3M	3415-0000 with ears
Flat Crimp	3M	3415-0000 with ears
	AMP	88083-1
	Ansley	609-5015
	SAE	SD6750 Series
Female, Soldered	AMP	2-583485-6
	Viking	3VH25/1JV5
	TI	H312125
Female, Wirewrap	TI	H311125
	Viking	3VH15/1JND5
	ITT Cannon	EC4A050A1A

Line Drivers and Terminators

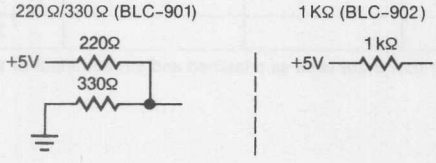
I/O Drivers — The following line drivers and terminators are all compatible with the I/O driver sockets on the BLX-350.

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note: I = Inverting, NI = Non-Inverting, OC = Open Collector

Port 1 has 25 mA totem pole drivers and 1 kΩ terminators.

I/O Terminators — 220Ω/330Ω divider or 1 kΩ pull-up.



Physical

Width: 2.85 in. (7.24 cm)
Length: 3.70 in. (9.40 cm)
Height:*
BLX-350 Board
0.80 in. (2.04 cm)
BLX-350 Board plus Host
1.13 in. (2.86 cm)
Weight: 1.79 oz. (51 gm)

*See Figure 2

Electrical Characteristics

DC Power Requirements

+5V @ 320 mA
Sockets XU3, XU4, XU5, and XU6 empty (as shipped).
+5V @ 500 mA
Sockets XU3, XU4, XU5, and XU6 contain 7438 buffers.
+5V @ 620 mA
Sockets XU3, XU4, XU5, and XU6 contain BLC-901 termination devices

Environmental

Operating Temperature:
0°C to 55°C
Relative Humidity: 0% to 90% non-condensing

Ordering Information

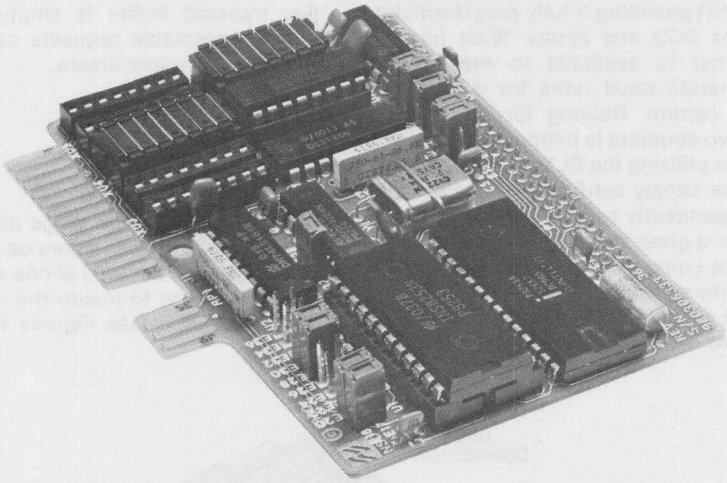
BLX-350	Parallel I/O Expansion Module

Documentation

420306332-001	BLX-350 Parallel I/O Expansion Module User's Manual

National Semiconductor

BLX-351
Serial I/O Expansion Module



- **BLX bus compatible I/O expansion**
- **Programmable synchronous/ asynchronous communications channel with RS232C or RS449/442 interface**
- **Software programmable baud rate generator**
- **Two programmable 16-bit BCD or binary timers/event counters**
- **Four jumper selectable interrupt request sources**
- **Accessed as I/O port locations**
- **Low power requirements**
- **Single +5V when configured for RS449/442 interface**
- **BLX bus on-board expansion eliminates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-351 Serial I/O Expansion Module is a member of the new line of BLX bus compatible expansion module products from National Semiconductor Corporation. The BLX-351 plugs directly into any BLX bus compatible host board offering incremental on-board I/O expansion. The BLX-351 module provides one RS232C or RS449/442 programmable synchronous/asynchronous communications channel with software selectable baud rates. Two general purpose programmable 16-bit BCD or binary timers/event counters are available to the host board to generate accurate time intervals under software control. The BLX board is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance and frees Multibus system traffic for other system resources. In addition, incremental power dissipation is minimal, requiring only 3.3 watts (assumes RS232C interface).

Functional Description

Communications Interface

The BLX-351 module uses the 8251A Universal Synchronous / Asynchronous Receiver / Transmitter (USART) providing one programmable communications channel. The USART can be programmed by the system software to individually select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e. synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The command lines, serial data lines, and signal ground lines are brought out to a double edge connector configurable for either an RS232C

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or RS449/442 interface (see Figure 3). In addition, the BLX-351 module is jumper configurable for either point-to-point or multidrop network connection.

16-Bit Interval Timers

The BLX-351 module uses an 8253 Programmable Interval Timer (PIT) providing 3 fully programmable and independent BCD and binary 16-bit interval timers. One timer is available to the system designer to generate baud rates for the USART under software control. Routing for the outputs from the other two counters is jumper selectable to the host board. In utilizing the BLX-351 module, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given baud rate or time delay is needed, software commmands the programmable timers to select the desired function. The functions of the timers are shown in Table 1. The contents of each counter may be read at any time during system operation.

Interrupt Request Lines

Interrupt requests may originate from four sources. Two interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the host board (i.e. receive buffer is full) or a character has been transmitted (i.e. transmit buffer is empty). In addition, two jumper selectable requests can be generated by the programmable timers.

Installation

The BLX-351 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 1 and 2).

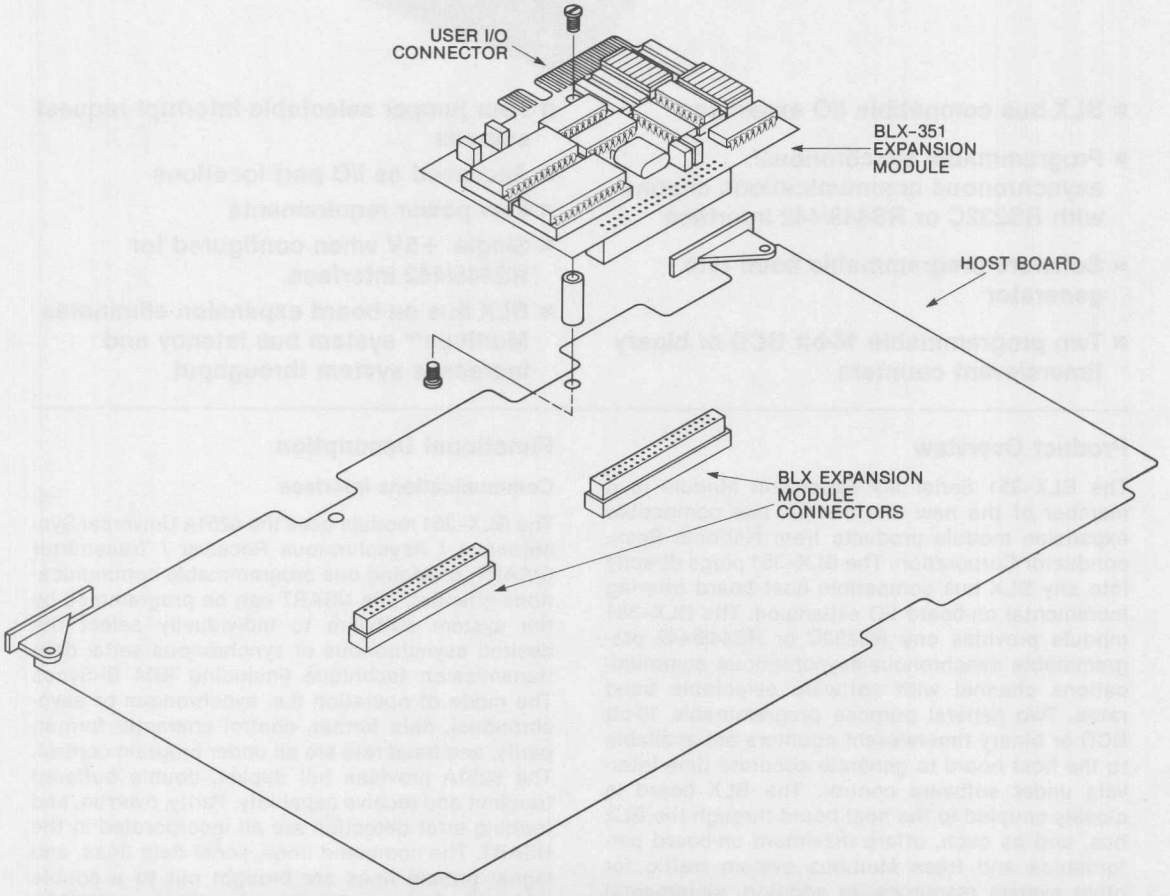


Figure 1. Installation of BLX-351 Module on a Host Board

Table 1. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Specifications

Word Size

Data — 8 bits

I/O Addressing

I/O Address	Chip Select	Function
X0, X2, X4, or X6	8251A USART	Write: Data Read: Data
X1, X3, X5, or X7		Write: Mode or Command Read: Status
X8 or XC	8253 PIT	Write: Counter 0 Load Count ÷ N) Read: Counter 0
X9 or XD		Write: Counter 1 (Load Count ÷ N) Read: Counter 1
XA or XE		Write: Counter 2 (Load Count ÷ N) Read: Counter 2
XB or XF		Write: Control Read: None

NOTE: The first digit of each port I/O address is listed as "X" since it will change depending on the type of host BLC microcomputer used. Refer to the Hardware Reference Manual for your host microcomputer to determine the first digit of the I/O address.

Access Time

Read — 250 ns max.

Write — 300 ns max.

Note: Actual transfer speed is dependent upon the cycle time of the host microcomputer.

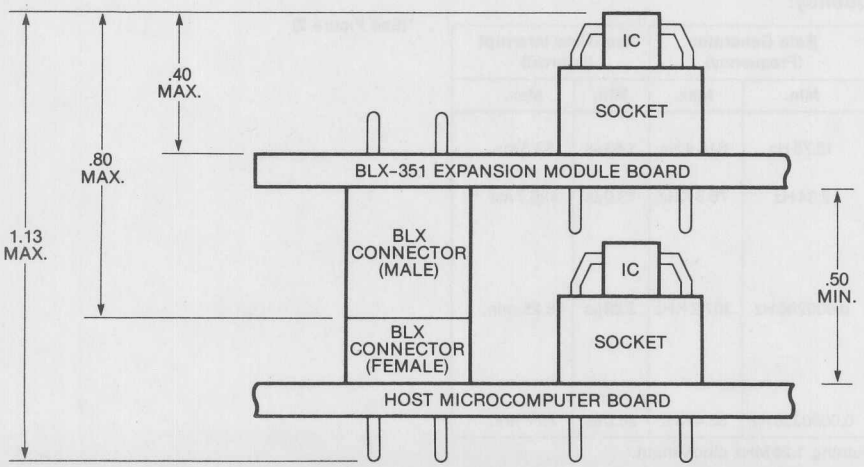


Figure 2. BLX-351 Expansion Module Mounting Clearance (Inches)

Serial Communications

Synchronous — 5-8-bit characters; internal character synchronization; automatic sync insertion; even, odd or no parity generation/detection.

Asynchronous — 5-8-bit characters; break character generation and detection; 1, 1½, or 2 stop bits; false start bit detection; even, odd or no parity generation/detection.

Sample Baud Rate:

8253 PIT Frequency[1] (KHz, Software Selectable)	8251A USART Baud Rate (Hz)[2]		
	Synchronous	Asynchronous	
		÷16	÷64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

Note 1: Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

Note 2: Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 KHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as frequency divider).

Interval Timer and Baud Rate Generator

Input Frequency (selectable):

1.23 MHz ± 0.1% (.813 μs period nominal)

153.6 KHz ± 0.1% (6.5 μs period nominal)

Output Frequency:

	Rate Generator (Frequency)		Real-Time Interrupt (Interval)	
	Min.	Max.	Min.	Max.
Single Timer[1]	18.75 Hz	614.4 Hz	1.63 μs	53.3 ms
Single Timer[2]	2.34 Hz	76.8 KHz	13.0 μs	426.7 ms
Dual Timer[3] (Counters 0 and 1 in series)	0.000286 Hz	307.2 KHz	3.26 μs	58.25 min.
Dual Timer[4] (Counters 0 and 1 in series)	0.0000358 Hz	38.4 KHz	26.0 μs	7.77 hrs.

Note 1: Assuming 1.23 MHz clock input.

Note 2: Assuming 153.6 KHz clock input.

Note 3: Assuming Counter 0 has 1.23 MHz clock input.

Note 4: Assuming Counter 0 has 153.6 KHz clock input.

Interrupts

Interrupt requests may originate from the USART (2) or the programmable timer (2).

Interfaces

BLX bus — all signals TTL compatible

Serial — configurable for EIA Standards RS232C or RS449/422

EIA Standard RS232C signals provided and supported:

- Clear to Send (CTS)
- Data Set Ready (DSR)
- Data Terminal Ready (DTR)
- Request to Send (RTS)
- Receive Clock (RXC)
- Receive Data (RXD)
- Transmit Clock (DTE TXC)
- Transmit Data (TXD)

EIA Standard RS449/422 signals provided and supported:

- Clear to Send (CS)
- Data Mode (DM)
- Terminal Ready (TR)
- Request to Send (RS)
- Receive Timing (RT)
- Receive Data (RD)
- Terminal Timing (TT)
- Send Data (SD)

Physical

Width: 2.85 in. (7.24 cm.)

Length: 3.70 in. (9.40 cm)

Height*: BLX-351 Board 0.80 in. (2.04 cm.)

BLX-351 Board and Host Board 1.13 in. (2.86 cm)

Weight: 1.79 oz. (51 gm.)

*(See Figure 2)

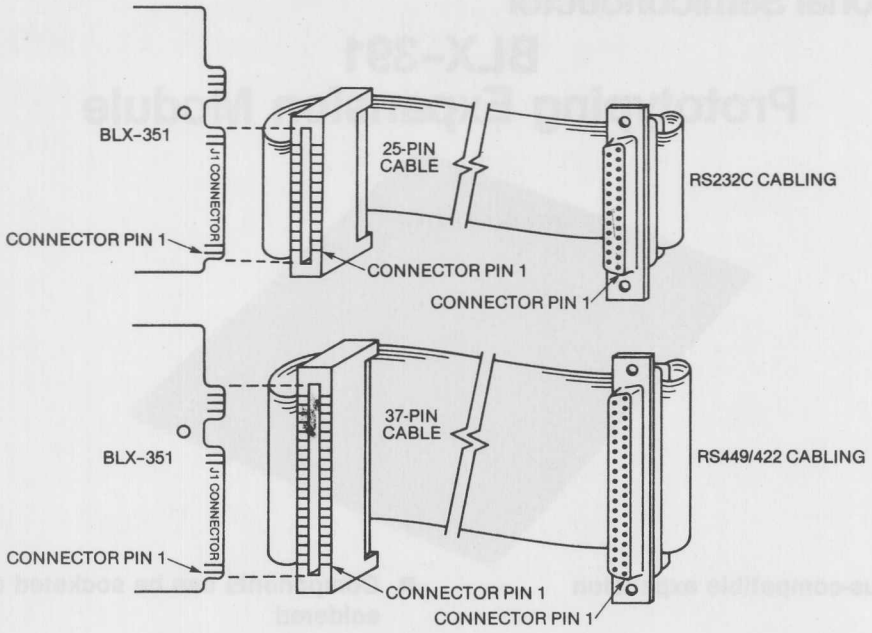


Figure 3. Cable Construction and Installation for RS232C and RS449/422 Interface

Serial Interface Connectors

Configuration	Mode[2]	Expansion Module Edge Connector	Cable	Connector
RS232C	DTE	26-pin[5], 3M-3642-0001	3M[3]-3349/25	25-pin[7], 3M-3482-1000
RS232C	DCE	26-pin[5], 3M-3642-0001	3M[3]-3349/25	25-pin[7], 3M-3483-1000
RS449	DTE	40-pin[6], 3M-3464-0001	3M[4]-3349/37	37-pin[1], 3M-3502-1000
RS449	DCE	40-pin[6], 3M-3464-0001	3M[4]-3349/37	37-pin[1], 3M-3503-1000

Note 1: Cable housing 3M-3845-4000 may be used with the connector.
Note 2: DTE — Data Terminal mode (male connector), DCE — Data Set mode (female connector).
Note 3: Cable is tapered at one end to fit the 3M-3462 connector.
Note 4: Cable is tapered to fit 3M-3464 connector.
Note 5: Pin 26 of the edge connector is not connected to the flat cable.
Note 6: Pins 37, 39, and 40 of the edge connector are not connected to the flat cable.
Note 7: May be used with cable housing 3M-3485-1000.

Electrical Characteristics

DC Power Requirements

Mode	Voltage	Amps (Max.)
RS232C	+5V ± 0.25V	460 mA
	+12V ± 0.6V	30 mA
	−12V ± 0.6V	30 mA
RS449/422	+5V ± 0.25V	530 mA

Environmental

Temperature — 0 to 55°C
Humidity — 0% to 90%, noncondensing

Ordering Information

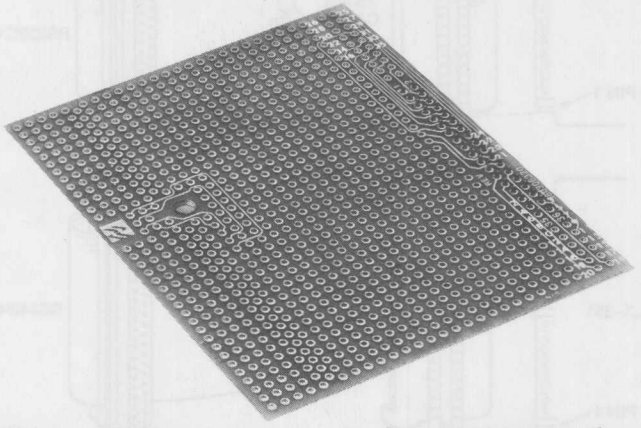
BLX-351 — Serial I/O Expansion Module

Documentation

420306333-001 — BLX-351 Serial I/O Expansion Module User's Manual

National Semiconductor

BLX-391
Prototyping Expansion Module



- **BLX bus-compatible expansion**
- **Permits easier user construction of custom circuitry for BLX/BLC systems**
- **Capacity for up to fourteen 16-pin equivalent integrated circuits**
- **Components can be socketed or flow soldered**
- **Provisions for right-angle card edge connectors can accommodate up to 120 pins for user-defined I/O**
- **BLX bus on-board expansion eliminates Multibus™ system bus latency and increases system throughput**

Product Overview

The BLX-391 Prototyping Expansion Module is a member of the new line of BLX bus-compatible expansion module products from National Semiconductor Corporation. The BLX-391 plugs directly into any BLX bus-compatible host board offering low cost incremental on-board expansion capabilities. As a result, any BLX bus-compatible host board may be expanded to perform any function that a user can incorporate onto a single-size (2.85″ × 3.70″) board. The BLX-391 can accomodate up to fourteen 16-pin equivalent integrated circuits, which can either be soldered or socketed. Wire-wrapping is accomplished on the component side of the board with individual wire-wrap pins or with wire-wrap strips. Card edge connectors are application-dependent, so provision is made to accomodate right angle connectors up to 120 pins. The BLX expansion module is closely coupled to the host board through the BLX bus, and as such, offers maximum on-board performance and frees Multibus system traffic for other system resources. The BLX-391 comes in kit form, providing the bare printed circuit board, a male BLX connector, and nylon mounting hardware.

Functional Description

The BLX-391 Prototyping Expansion Module is a general purpose prototyping printed circuit board, of traditional design, which meets the BLX single-size (2.85″ × 3.70″) form factor. A male BLX connector is included to allow connection to a BLX bus-compatible, Series/80 host board consistent with the design criteria followed on the entire family of BLX expansion module products.

BLX Bus

The BLX bus interface provided on BLX bus-compatible Series/80 host boards conforms to those signals listed in Table 1. With the exception of several signals (such as MPST/—Module Present), all signals are merely extensions of the microprocessor bus, and, as such, meet the specifications for that microprocessor. The custom circuitry must be designed to be compatible with the actual BLX bus interface on the BLX bus-compatible Series/80 host board being used. (Any questions concerning the BLX bus should be addressed to your local Field Applications Engineer.)

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Wire-Wrap

All wire-wrapping is accomplished on the component-side of the BLX-391 in order to remain within the envelope defined for the BLX expansion module family (see Figure 3). This necessitates the use of wire-wrap pins or strips. Recommended sizes and suitable vendors are provided in the specifications.

I/O Connector

Since the card edge I/O connector will differ with each application, only provision for a user-specified connector is offered. To remain within the envelope defined for the BLX expansion module family, the appropriate right angle connectors are suggested for all designs. Recommended sizes and suitable vendors are provided in the specifications.

Installation

The BLX-391 module plugs directly into either of the female BLX connectors on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figure 1 and Figure 2).

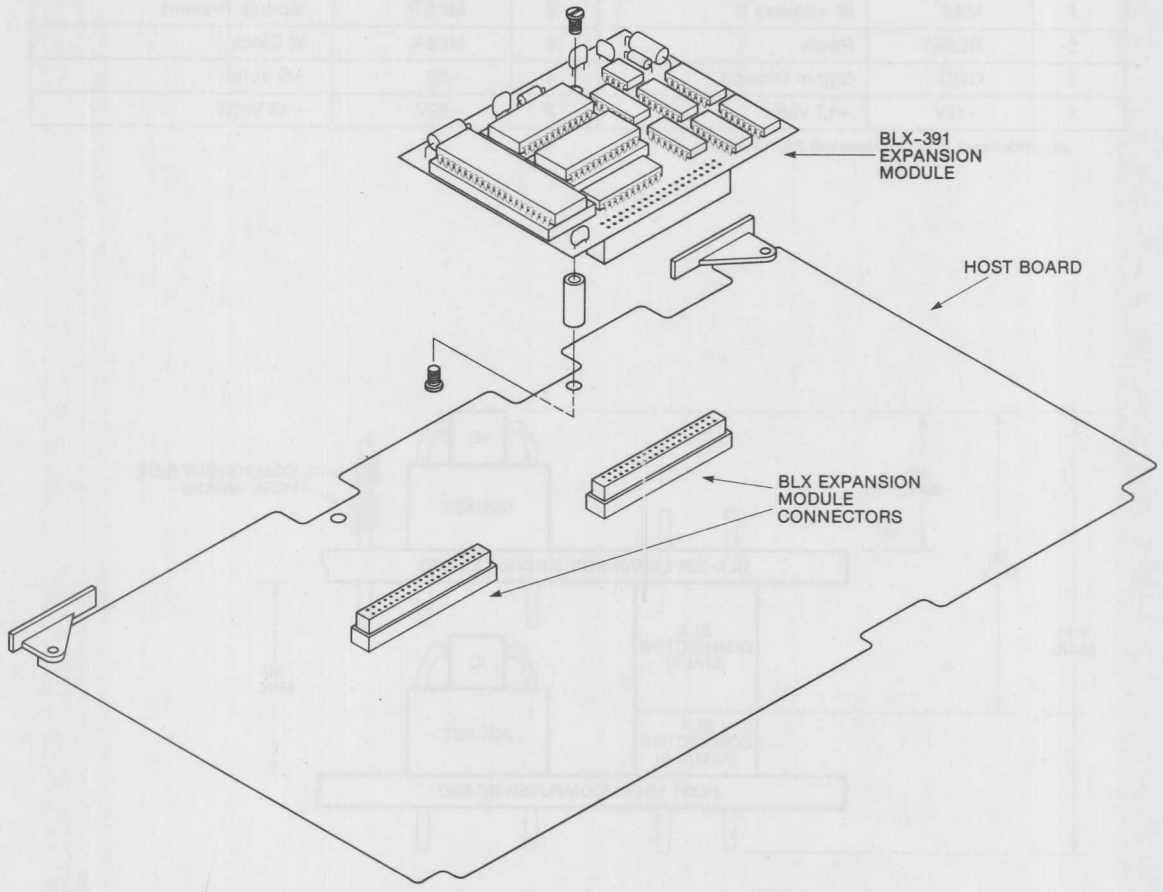


Figure 1. Installation of BLX-391 Module on a Host Board

31	MD1	MDATA Bit 1	32	MDACK/	M DMA Acknowledge
29	MD2	MDATA Bit 2	30	OPT0	Option 0
27	MD3	MDATA Bit 3	28	OPT1	Option 1
25	MD4	MDATA Bit 4	26	TDMA	Terminate DMA
23	MD5	MDATA Bit 5	24		Reserved
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20	MCS1/	M Chip Select 1
17	GND	Signal Ground	18	+5V	+5 Volts
15	IORD/	I/O Read Command	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Command	14	MINTR0	M Interrupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10		Reserved
7	MA2	M Address 2	8	MPST/	Module Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Ground	4	+5V	+5 Volts
1	+12V	+12 Volts	2	−12V	−12 Volts

All undefined pins are reserved for future use.

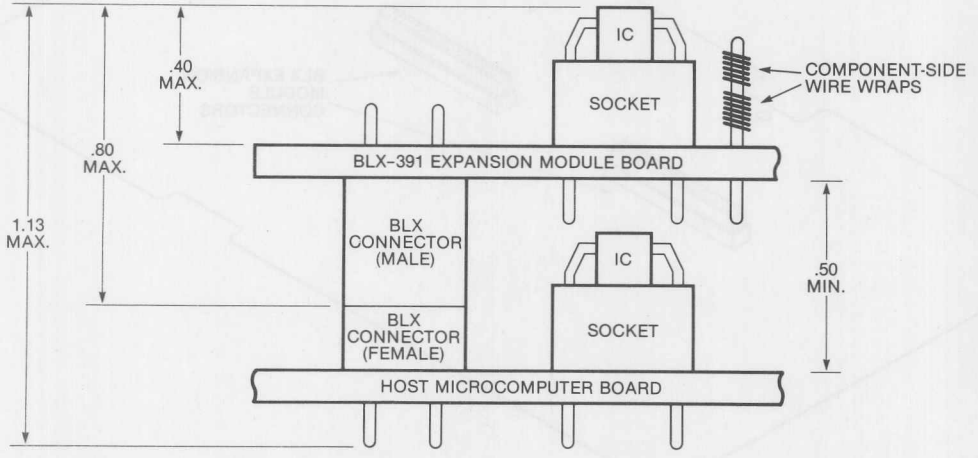


Figure 2. BLX-391 Expansion Module Mounting Clearances (inches)

Specifications

Wire-Wrap Hardware —

Sockets: Dual-in-line, low profile, on 0.10″ centers. Use the following (or equivalent):

Wire-Wrap Strips: Strips with pins on 0.10″ centers, with height above the board not to exceed 0.40″. Use the following (or equivalent):

Circuit Assembly Corp.
CA-536SP100-230-430

Wire-Wrap Pins: 0.40″ length max. Use the following (or equivalent):

Berg Electronics 65474-004

Connectors —

Right-angle connector on 0.10″ centers (board side). Use the following (or equivalent):

Circuit Assembly Corp.

Plugs
26-pin: CA-D26RSP100-230-090
50-pin: CA-D50RSP100-230-090

Sockets
26-pin: CA-26-IDS
50-pin: CA-50-IDS

Environmental

Operating Temperature: 0°C to 55°C

Relative Humidity: 0% to -90%, noncondensing

Physical

Height: 2.85 in. (7.24 cm)

Width: 3.70 in. (9.40 cm)

Depth:

BLX-391 with circuitry installed
0.80 in. (2.04 cm)

BLX-391 with circuitry + host board
1.13 in. (2.86 cm)

Weight: 1 oz. (28.35 gm)

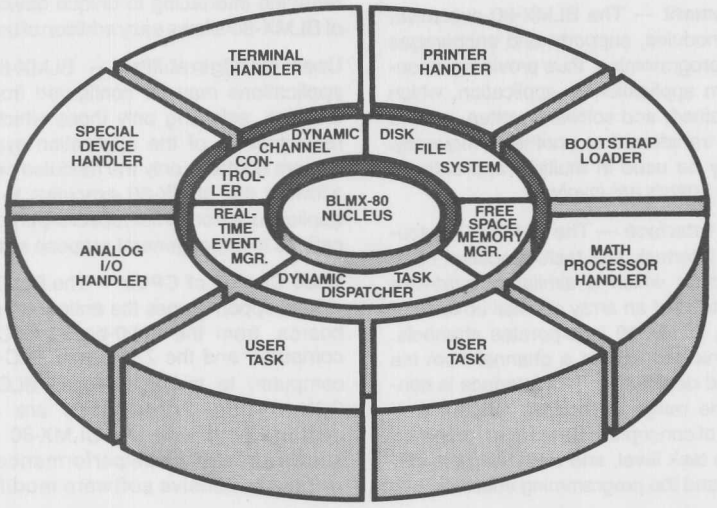
Order Information

BLX-391	Prototyping Expansion Module with BLX connector, nylon mounting hardware, and design aids.

Section 3
Board Level
Operating Systems

National Semiconductor

BLMX-80
Board-Level, Multitasking Executive



- **Configurability**
  - Fully user configurable
  - Menu selection procedure
  - Hardware independent
- **Compatibility**
  - 8080/8085, Z80®
  - Bus-like structure
- **Reliability**
  - Small, efficient nucleus
  - Simple user interface
  - Standard data structures
- **User-Oriented Support**
  - Extensive I/O handlers
  - Analog handlers
  - Disk file system
- **Easy-to-Use**
  - Prompting menus guide system configuration
  - Comprehensible system functions
  - Functional similarity for internal & external calls
  - Re-configurable

Product Overview

The BLMX-80 software system is a real-time, multitasking executive, specifically designed for use with National Semiconductor Corporation's Board Level Computer (BLC) products. It has been optimized for real-time applications such as process control, manufacturing monitoring, and data acquisition systems. The BLMX-80 executive is fully modular and can readily be configured to suit applications needs. It is completely hardware and location independent, thereby providing a fundamental base upon which users can build a wide range of application systems. In addition, BLMX-80 provides a bus-like structure which helps to integrate software with its underlaying hardware through predefined data structures and interconnect procedures. This concept of software-bus architecture insures maximum quality of standardization for compatibility and future expandibility.

The BLMX-80 nucleus requires only 512 bytes of RAM and 2K bytes of ROM. The system contains all major real-time functions including task scheduling, intertask communication and synchronization, interrupt handling and I/O control, as well as many optional features.

The Series/80 CPU boards supported by BLMX-80 include: BLC-80/05, BLC-80/10, BLC-80/11, BLC-80/12, BLC-80/14, BLC-80/11A, BLC-80/12A, BLC-80/14A, BLC-80/116, BLC-80/204, BLC-80/316, and BLC-8715. Support is guaranteed for all future CPU boards with an 8-bit microprocessor.

The peripheral I/O devices and controllers supported by BLMX-80 include: RS232 terminal, teletype terminal, Centronics printer, BLC-711, BLC-724, BLC-732, and BLC-8737 analog I/O boards, and more.

In-System Emulator is a trademark of National Semiconductor Corp.

Features

The BLMX-80 Board-Level, Multitasking Executive provides users of Series/80 products simple, easy-to-use, yet comprehensive, tools for creating a wide range of applications. The most notable features of BLMX-80 are:

Structured Environment — The BLMX-80 executive, and its associated modules, supports and encourages modular, structured programming, thus providing a consistent structure from application to application, which allows experience gained, and software written, on one system to be easily transferred to another. Frequently, entire programs may be used in multiple applications, *even if different CPU boards are involved.*

Hardware-Oriented Interface — The BLMX-80 executive provides for an intertask and task/executive communications architecture which is similar to hardware communications. Instead of an array of "mail boxes" (or "message centers"), BLMX-80 incorporates channels. One merely communicates across a channel from his module to the desired destination. This interface is consistent throughout the range of facilities offered, thus reducing the number of concepts to be learned, providing greater control at the task level, and increasing the efficiency of the system and the programming effort.

Library Modules — The BLMX-80 executive is constructed in a thoroughly modular manner with the full range of facilities being offered in multiple library modules, allowing easy selection of the exact facilities required.

Small Nucleus — The BLMX-80 nucleus was hand-coded in assembly language, versus being the output of a compilation of intermediate or high-level language. The resulting product is therefore smaller, and allows the incorporation of more features within the size generally accepted as optimum.

Priority Oriented Scheduler — The BLMX-80 scheduler insures that the highest priority task which is ready to execute is given control, allowing the system to be responsive to its external world. Dynamic reprioritization of tasks is supported for the most sophisticated of multitasking systems.

Real-Time Speed — Since BLMX-80 was hand-coded in assembly language, several advantages with regard to speed are gained. Task swapping, channel and message management, and I/O interfacing are executed much quicker than could be expected of a system written in a higher level language.

Direct Interrupt Processing — The BLMX-80 architecture employs interrupt channels which allow device-specific interrupt handling routines to interface directly with the interrupt source. This accomplishes servicing of interrupts without the overhead of task swapping, yet allows the operating system to maintain the integrity of the system. Combining this interrupt service architecture with a device-efficient nucleus results in an operating system that better supports demanding, real-time applications.

Comprehensive I/O Support — The BLMX-80 libraries contain support for a wide variety of I/O boards within the Series/80 product line, thus simplifying the addition of peripherals to an application system. For applications requiring interfacing to unique devices, the architecture of BLMX-80 allows easy addition of user-written handlers.

User Configurability — BLMX-80 executive-based applications may be configured from a wide range of facilities, selecting only those which meet the specific requirements of the application system. The resultant system contains only the modules necessary for its use, allowing the BLMX-80 executive to fit a wide range of applications from small, special-purpose, dedicated applications to large, general-purpose systems.

Wide Choice of CPUs — The BLMX-80 executive provides support across the entire range of Series/80 CPU boards, from the 8080-based BLC-80/11 board-level computer, and the Z80-based BLC-80/316 board-level computer, to the 8085-based BLC-80/05 and future CPU boards. Applications are offered an easy upgrade path with the BLMX-80 Executive, which allows greater price/performance to be achieved without expensive software modification.

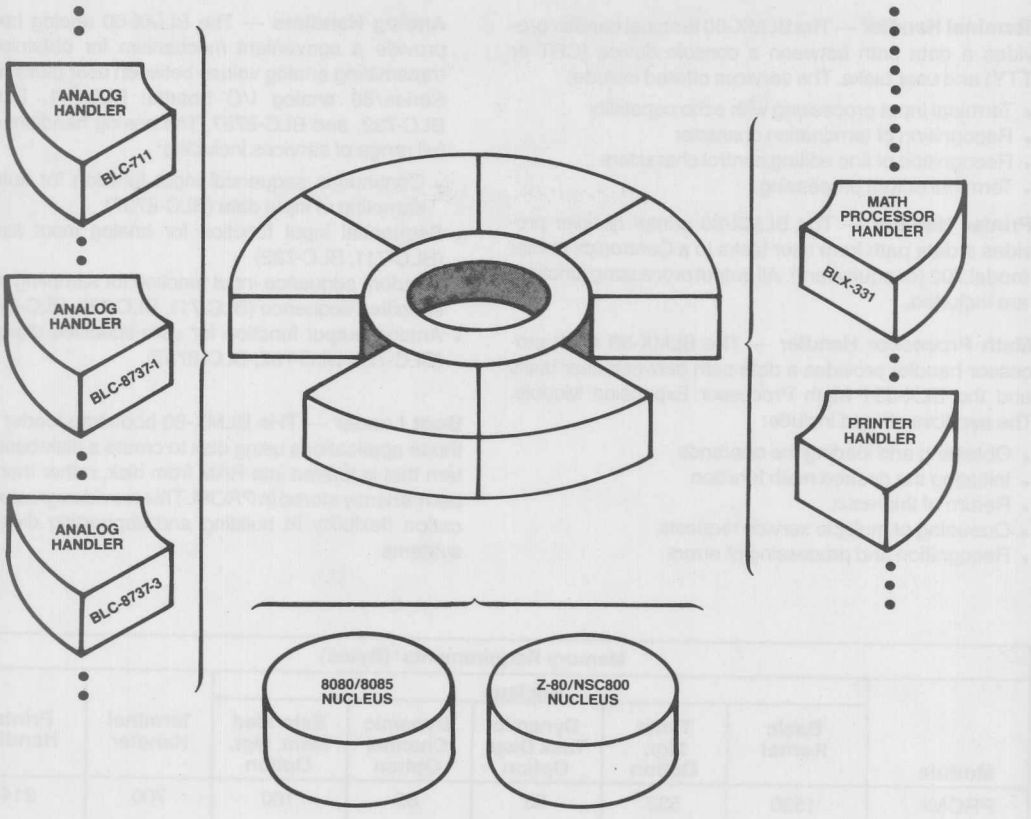
Event Driven — In the BLMX executive, each user task exists in its own "closed environment" — a virtual processor. Each virtual processor can synchronize with external/internal occurences through events. BLMX-80 supports a wide variety of events including: synchronization with task activities, external device operations, and the real-time clock.

Free Space Manager — The BLMX-80 executive has an integral free space manager. This feature not only reduces the amount of RAM required in an application system (potentially reduces board count), but also allows active modules more buffer area within any given space constraint.

Time-Of-Day Clock — The BLMX-80 executive has an integral system/time-of-day clock. Included is a real-time clock configurable to a resolution of ten milliseconds. This negates the need to allocate the extra memory required for these features which are necessary in most application systems.

Debugging Aids — The BLMX-80 executive has an user-oriented, interactive, software debugging aid. The debugger allows memory examination and modification, execution breakpoints, automatic stack overflow monitoring, and numerous other features which allow simplified task debugging and faster application system development.

Hardware/Software Compatibility — The user of BLMX-80 is guaranteed that his Series/80 boards and his BLMX-80 device handlers will always be compatible. If changes are necessitated on any item supported by National Semiconductor Corporation, the BLMX-80 user is guaranteed that no compatibilty problems will arise.



Configuration Flexibility Provides Application Freedom.
The BLMX-80 executive, and associated modules, allows the designer the freedom to choose from a wide range of Series/80 CPU, expansion, and peripheral controller boards upon which the application may be built. It allows you to break the ties between the application and the hardware, and thereby gain application freedom and save software development costs.

Facilities

The various facilities offered by the BLMX-80 executive are provided as independent library modules, thus allowing simple inclusion or exclusion depending on the user's specific requirements. These facilties are described below:

Nucleus — The BLMX-80 executive provides nuclei for operation on all Series/80 board-level computers. The nuclei provide real-time scheduling, interrupt handling, intertask communications, task control, free-space management, and time-of-day. The services offered are:

- Task message sending/receiving and synchronization
- External input/output and synchronization
- Task management
- Time control
- Creation and disposal of tasks during run time
- Extended free memory pool management (user space) with granularity control for optimization

STARPLEX is a trademark of National Semiconductor Corp.

Disk File System — The BLMX-80 disk file system provides for the filing and retrieving of data using disks. The system allows for either STARPLEX™ Development System Operating System compatible media format, or a user-specified format. The disk file system offers the following services in a STARPLEX Operating System compatible media format:

- Open/close a file for I/O operation
- Obtain I/O information and check I/O status
- Read/write data to/from a file
- Directory maintenance and attribute control
- Define user logical I/O error handler.
- Error detection

For those applications which require unique media formats, the BLMX-80 executive offers a level of processing which allows complete user flexibilty in formatting data. The services offered are:

- Format diskette tracks
- Perform diskette I/O operations
- Interface to disk controller.

Terminal Handler — The BLMX-80 terminal handler provides a data path between a console device (CRT or TTY) and user tasks. The services offered include:

- Terminal input processing with echo capability
- Recognition of termination character
- Recognition of line editing control characters
- Terminal output processing.

Printer Handler — The BLMX-80 printer handler provides a data path from user tasks to a Centronics printer model 702 (or equivalent). All output processing functions are included.

Math Processor Handler — The BLMX-80 math processor handler provides a data path between user tasks and the BLX-331 Math Processor Expansion Module. The services offered include:

- Obtaining and loading the operands
- Initiating the desired math function
- Return of the result
- Queueing of multiple service requests
- Recognition and processing of errors

Analog Handlers — The BLMX-80 analog handlers provide a convenient mechanism for obtaining and transmitting analog values between user tasks and the Series/80 analog I/O boards: BLC-711, BLC-724, BLC-732, and BLC-8737. The analog handlers offer a full range of services including:

- Continuous sequential input function for automatic sampling of input data (BLC-8737)
- Sequential input function for analog input sampling (BLC-711, BLC-732)
- Random sequence input function for sampling at user-specified sequence (BLC-711, BLC-732, BLC-8737)
- Analog output function for user-specified digital data (BLC-724, BLC-732, BLC-8737).

Boot Loader — THe BLMX-80 bootstrap loader allows those applications using disk to create a disk-based system that is loaded into RAM from disk, rather than being permanently stored in PROM. This provides greater application flexibility in building and supporting disk-based systems.

Memory Requirements[1] (Bytes)							
	Nucleus						
Module	Basic Kernel	Timer Mgr. Option	Dynamic Task Disp. Option	Dynamic Channel Option	Extended Mem. Mgr. Option	Terminal Handler	Printer Handler
PROM[2]	1530	532	53	83	180	700	214
RAM[3]	328	—	—	—	—	40	16

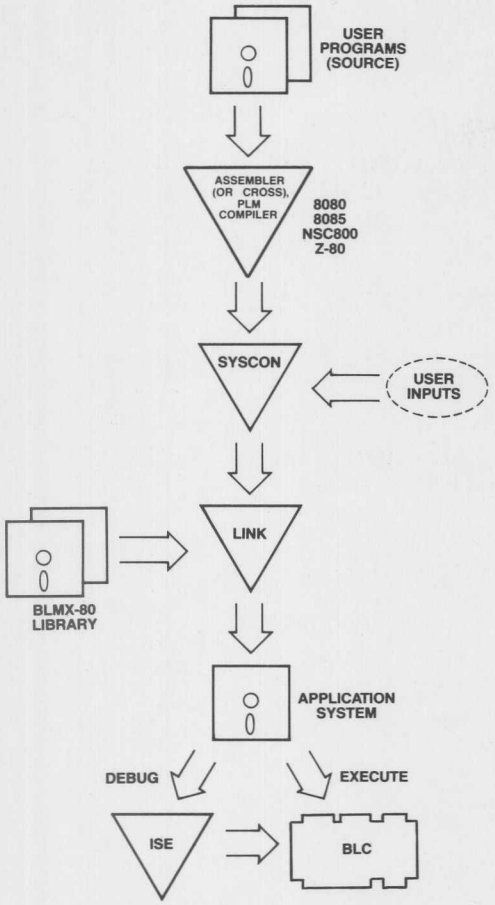
Module	Disk File System	Analog Handlers				Math Processor Handler	Bootstrap Loader
		BLC-711 Input	BLC-724 Output	BLC-732 I/O	BLC-8737 I/O		
PROM[2]	13300	157	84	228	261	500	700
RAM[3]	2000	48	20	68	68	80	400

Note:
1. All figures are approximate. Modules whose final size is user-dependent have the minimum requirements listed.
2. Indicates amount of code which can be configured in PROM.
3. Does not include user-defined Message Control Blocks.

BLMX-80 Memory Requirements.

The System Generation Process

The BLMX-80 system generation process is, for the most part, accomplished by running a program called SYSCON on a STARPLEX™ Development System. The user merely "fills out forms" presented on STARPLEX, answering questions concerning which Series/80 CPU board will be used, which library modules are required, location of handlers and user-generated tasks, and assignment of channels for communications between tasks and with the executive. The resulting files are then merged into object form executable on the application system. The system may then be debugged using the appropriate In-System Emulator (ISE™) from National Semiconductor Corporation, or the BLMX-80 interactive debugger. The final application system code is then available for either PROM or disk-based systems.



System Generation Process.
The user is guided through system generation by SYSCON. Sophisticated In-System Emulators from National Semiconductor Corporation take the pain out of debugging application-unique software.

Supported Hardware

Board-Level Computers

BLC-80/05	BLC-80/12A
BLC-80/10	BLC-80/14A
BLC-80/11	BLC-80/116
BLC-80/12	BLC-80/204
BLC-80/14	BLC-80/316
BLC-80/11A	

Mass Storage Controllers

BLC-8221	BLC-8222

Analog Boards

BLC-711	BLC-8737-1
BLC-724	BLC-8737-2
BLC-732	BLC-8737-3

Math Processor

BLX-331

BLMX-80 Executive Shipping Package

One diskette containing:

- BLMX-80 Nucleus
- Terminal Handler
- Printer Handler
- Disk File System
- Analog Handlers
- Math Processor Handler
- Interactive Debugger
- Bootstrap Loader
- SYSCON (System Configuration Program)

Reference Manuals

- BLMX-80 Reference Manual
- BLMX-80 System User's Manual

Order Information

BLMX-80AS	BLMX-80 Executive for 8080/8085-based, Series/80 CPU boards on a single density diskette.
BLMX-80AD	BLMX-80 Executive for 8080/8085-based, Series/80 CPU boards on a double density diskette.
BLMX-80BS	BLMX-80 Executive for Z80/Series/80 CPU boards on a single density diskette.

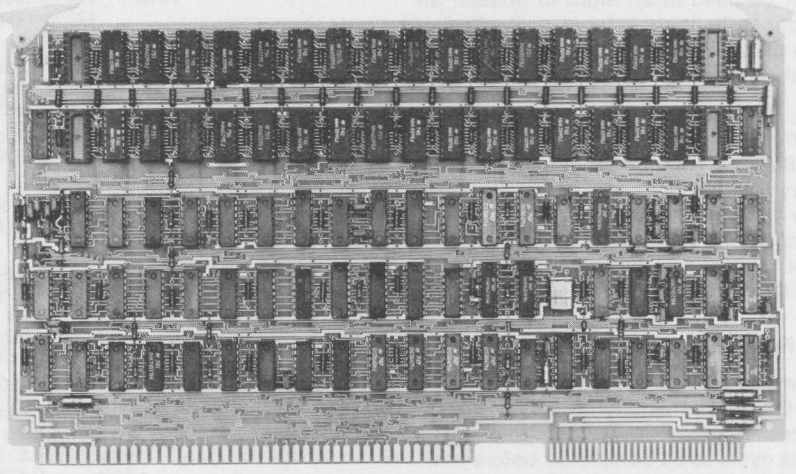
Documentation

420306431-001	BLMX-80 System Reference Manual
420306432-001	BLMX-80 System User's Manual

Section 4
Memory Expansion Boards

National Semiconductor

BLC-8016, BLC-048, and BLC-064 Ram Memory Boards



- **Flexible System Configuration**
  - BLC-8016 — 16K bytes
  - BLC-048 — 48K bytes
  - BLC-064 — 64K bytes
  - 8- or 16-bit data access
- **Enhanced System Performance**
  - On-board refresh and control logic
  - Synchronized (transparent) refresh capability — no refresh wait state with BLC-80/204
  - Auxiliary power bus and memory protect logic for battery backup requirements
- **Ease of Maintenance**
  - Socketed MM5290 16K × 1 or MM5298 8K × 1 dynamic RAMs
- **Fully Compatible with BLC/SBC Products**
  - Plug-replacements for BLC-016 and SBC-016/032/048/064

Product Overview

The BLC-8016, BLC-048 and BLC-064 RAM expansion boards are designed to meet large memory requirements without sacrificing space or significantly reducing available power. These boards provide 16K bytes, 48K bytes and 64K bytes, respectively, of dynamic random access read/write memory (RAM) on a single printed circuit board. The boards are complete with all refresh and control electronics, address and data buffers, and memory array.

Designed-in flexibility permits the user to obtain the optimum system configuration. Starting address segments are provided at 16K byte boundaries and data may be accessed in 8- or 16-bit modes. Memory may be expanded up to one megabyte in a single Series/80 system by using the BLC-064 and implementing logic to activate additional, existing address lines.

The BLC-8016, BLC-048 and BLC-064 are plug-compatible replacements for Intel's SBC-016, 048 and 064 and BLC-016, and plug directly into any BLC/SBC system.

Functional Description

The BLC-8016, -048 and -064 are based on National's MM5290 16K × 1-bit and MM5298 8K × 1-bit dynamic RAM modules. Memory access time is a fast 430 nanoseconds and a full read or write cycle takes only 660 nanoseconds. The memory comple-

ment is organized into independent 16K × 8-bit address blocks. Each block may be configured to a unique starting address on one of four 16K byte boundaries. In the case of the BLC-8016 and BLC-048, this allows the user greater flexibility when using other Series/80 System ROM/PROM memory or I/O boards.

The board can be used in an eight or sixteen bit data mode. A separate control signal on the Series/80 system bus provides data mode selection under system control.

The BLC-8016, -048 and -064 have a 20-bit address bus. This permits the sophisticated user to combine up to 16 BLC-064 RAM boards to create a megabyte memory system. Normally, 8080-based systems use only 16 of the 20 available address bits; however, board select logic may be enabled to allow a BLC-064 to occupy any one of sixteen 64K byte blocks within a megabyte address range.

Synchronized Refresh

On-board automatic refresh logic is used to refresh a portion of the total memory every 13 microseconds. Refresh logic waits for an in-process memory access cycle to be completed before initiating a refresh cycle. In addition there is a special status signal implemented on the BLC-80/204 microcomputer for refresh synchronization. When enable, this feature causes BLC-8016, -048 and -064 memory refresh cycles to synchronize with CPU activity and results in increased system throughput and consistent software timing loop results.

Memory Protect

Memory protection of RAM contents is provided through an auxiliary connector on the memory board. The logic connected to this line is TTL compatible and, when asserted as an active low from an external source, disables read and write access functions. This input is provided for the protection of RAM contents during a system power-down sequence.

Specifications

Memory Size —
BLC-8016 — 16K bytes
BLC-048 — 48K bytes
BLC-064 — 64K bytes

Word Size —
8 or 16 bits

Access Time —
430 ns

Cycle Times —
Read — 660 ns
Write — 660 ns (delayed write)
1230 ns (advanced write)
Refresh — 615 ns

Address Selection —
Jumper selection of contiguous 16K byte blocks starting at locations 0000_{16}, 4000_{16}, 8000_{16}, or $C000_{16}$

System Bus Connector —
Data, address and command signals are TRI-STATE® TTL compatible

System Bus Connector —
86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary Power —
Separate power bus provided for systems requiring battery backup of memory for critical applications. On-board jumpers provided to enable this mode of operation.

Power —
(BLC-048 and BLC-064)

	Operating	Battery
+5V	3.0A	1.7A
−5V	0.011A	0.011A
+12V	0.47A	0.140A

Environmental —
Temperature 0 °C to 55 °C
Humidity 0 to 90% non-condensing

Physical —

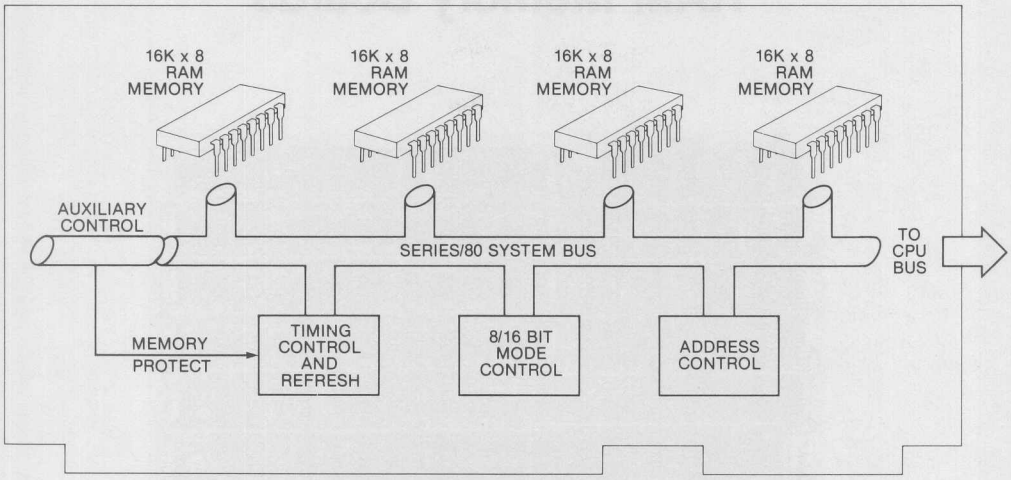
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-8016	16K Byte RAM board
BLC-048	48K Byte RAM board
BLC-064	64K Byte RAM board

Documentation

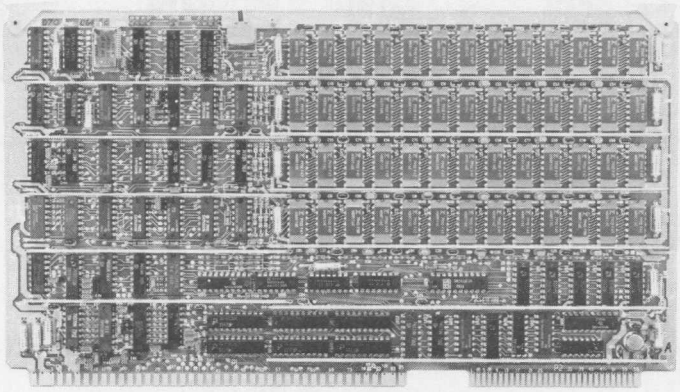
420305529-001	BLC-8016/048/064, 16K/48K/64K Byte RAM Board Hardware Reference Manual



BLC-064 System Diagram

National Semiconductor

BLC-8064 Family
RAM Memory Boards



- **New Features**
  - **Parity (error detection)**
  - **ECC (error correcting circuitry)**
- **Enhanced System Performance**
  - **On-board refresh and control logic**
  - **Synchronized (transparent) refresh capability**
  - **Auxiliary power bus and memory protect logic for battery backup requirements**
- **Compatible with all Series/80 boards and card cages**
- **Flexible System Configuration**
  - **48 K and 64 K bytes**
  - **RAM expansion for 8- or 16-bit systems**
  - **Flexible address strapping options**
- **Ease of Maintenance**
  - **Latching error indicator LED's isolate failed memory chip**
  - **All memory chips socketed**
  - **Error Status Register logs failures for CPU**

Product Overview

The BLC-8064 Family of RAM expansion boards are designed to meet large memory requirements which additionally must maintain high data integrity. The unique features of this series of boards includes parity and ECC (error correcting circuitry).

Parity is a method by which errors encountered during reading data from RAM may be detected. These can be caused by occurences as unpredictable as power supply noise/variations, computer system noise generation, noise/interference external to the computer system, or even alpha particle radiation. Upon discovering an error, the board notifies the CPU, so further actions will not take place with the known bad data.

ECC goes one step further. When a single-bit error (per 8-bit byte) is detected, it is automatically corrected. This is done with no loss in access time, so it is transparent to the CPU, except by monitoring the Error Status Register. Multiple-bit errors, per byte, are detected, (but not corrected) and then passed to the CPU via an interrupt or the Error Status Register. Calculations indicate that single-bit error correction provides significant improvement in reliability.

Functional Description

The BLC-8016A or B, 8032A or B, 8048 A or B and 8064A or B are based on the MM5290 16K×1 dynamic RAM chip. The board architecture is such that the BLC-8064 can be assigned any 64K byte page address within a one megabyte address space. The 16K, 32K, and 48K byte versions can occupy any 16K byte segment within any 64K byte page. This allows flexibility when using other Series/80 PROM or I/O boards in the system.

Error Status Register

Error condition information is stored in an on-board Error Status Register (ESR). This information is displayed by the on-board status LED indicators, which indicate a single or double bit error, and also indicate the chip row and column in which the error occurred. The entire contents of the ESR may be read by the host CPU. Jumper options provide memory system interrupts to be generated for single bit errors, double bit errors, or both.

The ESR, together with the LED's and interrupts, provide the user with several conveniences that enhance the manufacture, test, operation, and field support phases of a computer system.

Parity Option

This option is designated by an "A" suffix in the product number. It provides detection of odd numbers of bit errors through the use of an additional "parity" bit per 8-bit memory byte. The parity bit is set on the write cycle if there are an odd number of "ones" in the byte. It is again generated on a read cycle, and compared to the original value. If the two values do not match, a parity error is indicated through the Error Status Register and the LED indicators. At the user's option, the host CPU can be notified of this condition through any of the Multibus interrupts.

ECC Option

This option is designated by a "B" suffix in the product number. The ECC option expands the basic memory to include five additional bits for each byte. Each of the ECC bits is the parity of a subset of data bits, and is generated during a write operation, and the resultant compared to the stored values. The resulting "syndrome" bits indicate that either correct data was read, or that an error has occurred. In the event of a single bit error, the incorrect bit is identified and inverted before it is transfered to the Multibus, thus preserving the data integrity of the computer system. In the unlikely even that a multiple bit error occurred, the Error

Status Register and/or error interrupt make it possible for a user error recovery program to take the appropriate action.

The inherent factors of error correcting memory, together with the other board features, provide a virtually failure free memory system.

Refresh

On-board transparent refresh circuitry performs all necessary functions associated with maintaining the dynamic RAM contents. All refresh functions can be powered from either the Multibus or the auxiliary battery backup bus. Contention between the refresh function and normal read or write accesses are resolved with the refresh-read/write priority logic. A jumper option permits the refresh to be controlled externally by Series/80 CPU such as the BLC-80/204.

Battery Backup

The BLC-8064 family offers complete battery backup with several advantages. These include 1) low power drain enhanced by a special battery power bus used only by those components which are required for memory refresh, 2) a memory protect line which may be used to prevent spurious memory write cycles caused by random transient signals during power fail, and 3) the ablity to determine memory integrity after power fail by reading all memory locations and the Error Status Register via a user routine.

Specifications

Memory Size — Bytes With Parity With ECC

48K BLC-8048A
64K BLC-8064B

Word Size — 8 bits

Access Time — 400 ns

Cycle Times — Read — 500 ns
Write — 500 ns (delayed write)
700 ns (advanced write)
Refresh — 450 ns

Address Selection — Any 64 K byte page boundary for BLC-8064

Any 16 K byte boundary within 64 K byte page for BLC-8016, 8032, 8048

System Bus Connector — Multibus compatible — 86 contact, double-sided card edge connector on 0.156 inch centers

Recommended mating connectors:

CDC VPB01E43A00A1
Viking 2V43/1 and 5

Auxiliary Bus — 60 contact, double-sided card edge connector on 0.1 inch centers

Recommended mating connectors:

AMP PE5-14559
TI H311130

Power (BLC-8064B)

	Operating	Battery
+5 VDC	2.0 A	0.5 A
−5 VDC		0.05 A
+12 VDC	0.1 A	0.06 A
−12 VDC	0.001 A	

Environmental Temperature — 0°C to 55°C
Humidity — 0% to 90% non-condensing

Physical

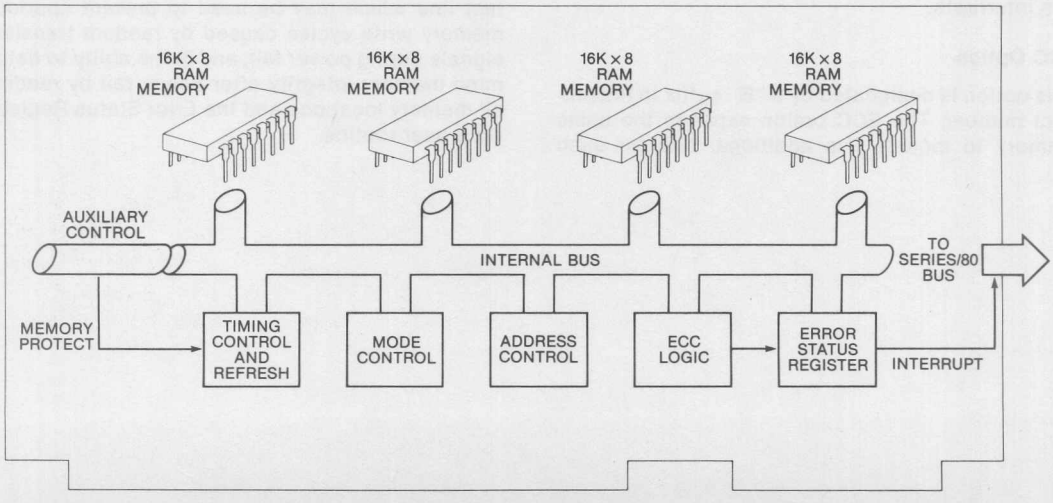
Height	6.75 in.	(17.15 cm.)
Width	12.00 in.	(30.48 cm.)
Depth	0.50 in.	(1.27 cm.)
Weight	16 oz.	(454 gm.)

Order Information

BLC-8048A	48 K Byte RAM Board with Parity
BLC-8064B	64 K Byte RAM Board with ECC

Documentation

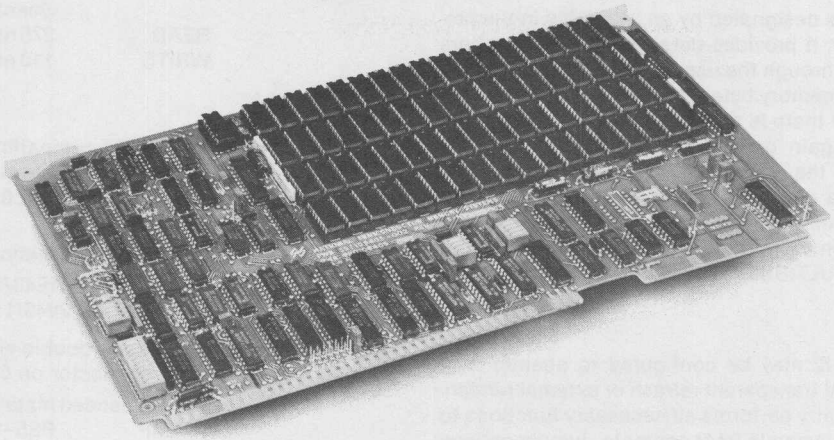
420306211-001	BLC-8064 Family RAM Expansion Board Hardware Reference Manual



BLC-8064B System Diagram

National Semiconductor

BLC-0512(A)
512K-Byte Memory Card Family



- **Features**
  - Parity (error detection)
  - Selectable parity interrupt
  - 512K bytes memory
- **Enhanced Systems Performance**
  - On-board refresh and control logic
  - Internal (transparent) refresh
  - Optional external refresh
  - Battery backup capability
- **MULTIBUS™ IEEE 796 Standard**
- **Compatible with all Series/80 Boards and Card Cages**
- **Flexible Systems Capability**
  - 8- or 16-bit data bus
  - 20- or 24-bit memory addressing
  - 8-, 12-, or 16-bit I/O addressing
- **Ease of Maintenance**
  - Control status register logs failures for CPU
  - All RAMs socketed

Product Overview

The BLC-0512 RAM memory cards are designed and tested to meet the users increasing memory requirements while maintaining a high level of data integrity. The card is available in 128, 256, 384 and 512K bytes of memory. The optional parity feature enhances data integrity.

Parity is a method to detect errors which may occur while reading data from the RAM. In the event a data error occurs the CPU is notified. Error information is also logged in the Control Status Register (CSR). Selectable parity interrupts allow the user to determine which interrupt request line is used. Any one of eight interrupt request lines may be selected.

Functional Description

The BLC-0512 is a 512K byte (512K × 8,9) random access memory card designed to be compatible with all Series/80 microcomputers. Utilizing the available options, the BLC-0512 is operational in a wide variety of configurations including 8-, 12-, or 16-bit I/O addressing. Set via a DIP switch, the starting address may be set on any 16K word boundary within the 16M byte range.

Control Status Register

Parity error information is stored in an on-board CSR. The CSR is a software addressable 16-bit Control Status Register. The CSR may be set to respond

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mode, it will respond to two consecutive byte addresses. By performing a minor jumper change, the CSR will operate with an 8-, 12-, or 16-bit I/O address.

Parity Option

This option is designated by an "A" suffix in the product number; it provides detection of odd numbers of bit errors through the use of an additional "parity" bit per 8-bit memory byte. The parity bit is set on the write cycle if there is an odd number of ones on the byte. It is again generated on a read cycle, and compared to the original value. If the two values do not match, a parity error is indicated through the Control Status Register. At the user's option, the host CPU can be notified of this condition through any of the MULTIBUS™ interrupts.

Refresh

The BLC-0512 may be configured to operate with either internal transparent refresh or external refresh. Refresh circuitry performs all necessary functions to maintain the dynamic RAM contents. Jumper options permit refresh to be controlled by the on-board circuitry or externally by many Series/80 CPUs.

Battery Backup

The BLC-0512 may be employed with battery back-up, utilizing +5V protected power. When battery back-up is used, in the event of a power outage, only the refresh circuitry is driven to maintain memory data. The low power drain assures maximum life of the battery back-up system.

Reliability

For increased reliability, the BLC-0512 is manufactured with A+ preconditioned IC's. After being debugged in a memory exerciser the cards are placed in a burn-in chamber and tested at 70°C for 72 hours. During this process the cards are subjected to a variety of bit patterns with extreme high and low voltage margining.

All errors are continuously logged and all failure locations are replaced with burned-in RAMs. The final 24 hours must be error free prior to completion of burn-in. All boards are then tested in a host system to verify full operational ability.

	MULTIBUS BLC-80 Series
Capacity	512 K Bytes (512 K × 9) Max.

Timing

	Access (max.)	Cycle (max.)
READ	275 ns	400 ns
WRITE	110 ns	400 ns

System Bus

Connection — MULTIBUS compatible — 86-contact, double-sided card edge connector on 0.156″ centers.

Recommended mating connectors:

CDC	VPB01E43A00A1
Viking	2V43/1 and 5

Auxiliary bus — 60-contact, double-sided card edge connector on 0.1″ centers.

Recommended mating connectors:

AMP	PE5-14559
TI	H311130

Power (512 K × 9)

$+5V_{DC}$	Max.	Typ.
Operating	3.6 A	3.2 A
Standby	3.4 A	3.2 A

Environmental

Temperature 0°C to 55°C

Relative Humidity 0 to 95% non-condensing

Physical

Depth: 0.49 in. (1.27 cm)

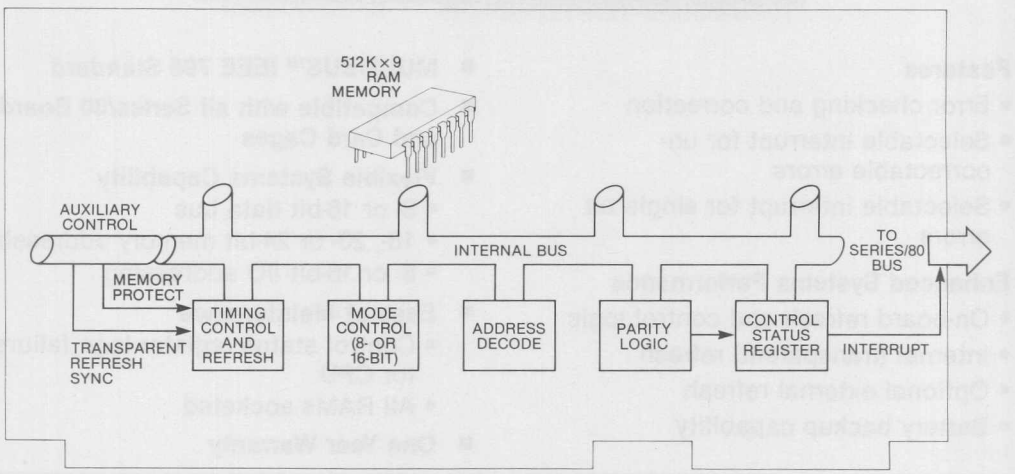
Width: 6.75 in. (17.15 cm)

Length: 12.00 in. (30.48 cm)

Order Information

Part Number	Memory	Parity
BLC-0128/64	128KB	No
BLC-0128A/64	128KB	Yes
BLC-0256	256KB	No
BLC-0256A	256KB	Yes
BLC-0384	384KB	No
BLC-0384A	384KB	Yes
BLC-0512	512KB	No
BLC-0512A	512KB	Yes
BLC-0512M	Technical Manual	

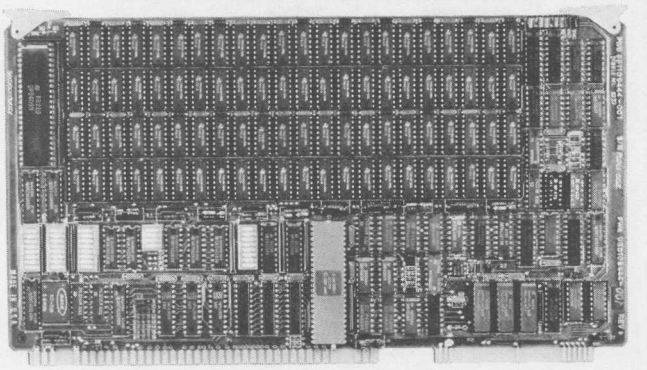
Warranty: One year parts and labor



BLC-0512 System Diagram

National Semiconductor

BLC-0512B
512K-Byte Memory Card Family



- **Features**
  - Error checking and correction
  - Selectable interrupt for uncorrectable errors
  - Selectable interrupt for single bit errors
- **Enhanced Systems Performance**
  - On-board refresh and control logic
  - Internal (transparent) refresh
  - Optional external refresh
  - Battery backup capability
- **MULTIBUS™ IEEE 796 Standard**
- **Compatible with all Series/80 Boards and Card Cages**
- **Flexible Systems Capability**
  - 8- or 16-bit data bus
  - 16-, 20- or 24-bit memory addressing
  - 8- or 16-bit I/O addressing
- **Ease of Maintenance**
  - Control status register logs failures for CPU
  - All RAMs socketed
- **One Year Warranty**

Product Overview

The BLC-0512B RAM memory cards are designed to meet the user's increasing memory requirements while maintaining a high level of data integrity. The card is available in 128, 256, 384, and 512K bytes of memory. The error correction feature enhances data integrity.

ECC is a method to detect and correct errors which may occur while reading data from the RAM. In the event a data error occurs, the CPU is notified. Error information is also logged in the Control Status Register (CSR). Selectable interrupts allow the user to determine which interrupt request line is used. Any two of eight interrupt lines may be selected. Single bit errors set one interrupt and double bit errors set a separate interrupt. Both may be assigned the same interrupt.

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Functional Description

The BLC-0512B is a 512K byte (256K x 22) random access memory card designed to be compatible with all Series/80 microcomputers. Utilizing the available options, the BLC-0512B is operational in a wide variety of configurations including 8- or 16-bit I/O addressing. Set via a DIP switch, the starting address may be set on any 4K byte boundary within the 16M byte range.

Control Status Register

ECC error information is stored in an on-board CSR. The CSR is a software addressable 16-bit Control Status Register. The CSR may be set to respond to 1 of 64,536 word addresses, or if operated in the byte mode, it will respond to two consecutive byte addresses. By performing a minor jumper change, the CSR will operate with an 8- or 16-bit I/O address.

Refresh

The BLC-0512B may be configured to operate with either internal transparent refresh or external refresh. Refresh circuitry performs all necessary functions to maintain the dynamic RAM contents. Jumper options permit refresh to be controlled by the on-board circuitry or externally by many Series/80 CPUs.

Battery Backup

The BLC-0512B may be employed with battery back-up, utilizing +5V protected power. When battery back-up is used, in the event of a power outage, only the refresh circuitry is driven to maintain memory data. The low power drain assures maximum life of the battery back-up system.

Reliability

For increased reliability, the BLC-0512B is manufactured with A+ preconditioned IC's. After being debugged in a memory exerciser, the cards are placed in a burn-in chamber and tested at temperature extremes for a liberal time period. During this process the cards are subjected to a variety of bit patterns with extreme high and low voltage margining.

All errors are continuously logged and all failure locations are replaced with burned-in RAMs. The final 24 hours must be error free prior to completion of burn-in. All boards are then tested in a host system to verify full operational ability.

Specifications

Compatibility
IEEE 796
MULTIBUS™
BLC-80 Series

Capacity
256K Words (256K × 22) Max.

Timing

	Access (max.)	Cycle (max.)
READ	350 ns	500 ns
WRITE WORD	110 ns	400 ns
WRITE BYTE	400 ns	500 ns

System Bus

Connection — MULTIBUS compatible — 86-contact, double-sided card edge connector on 0.156″ centers.

Recommended mating connectors:
CDC VPB01E43A00A1
Viking 2V43/1 and 5

Auxiliary bus — 60-contact, double-sided card edge connector on 0.1″ centers.

Recommended mating connectors:
AMP PE5-14559
TI H311130

Power (256K × 22)

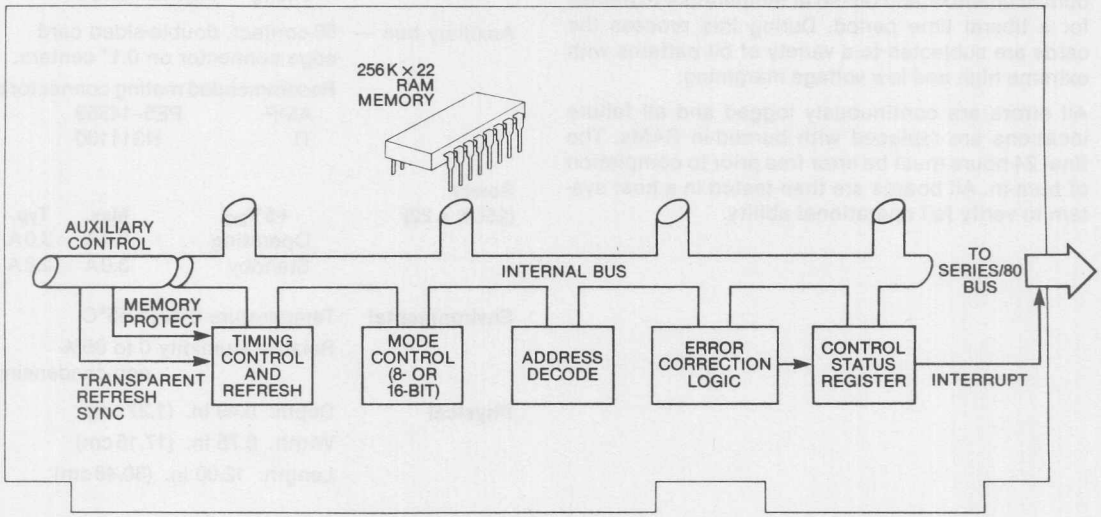
$+5V_{DC}$	Max.	Typ.
Operating	3.4A	3.0A
Standby	3.0A	2.8A

Environmental
Temperature 0°C to 55°C
Relative Humidity 0 to 95% non-condensing

Physical
Depth: 0.49 in. (1.27 cm)
Width: 6.75 in. (17.15 cm)
Length: 12.00 in. (30.48 cm)

256KB	BLC-0256B	BLC-0256BM
384KB	BLC-0384B	BLC-0384BM
512KB	BLC-0512B	BLC-0512BM

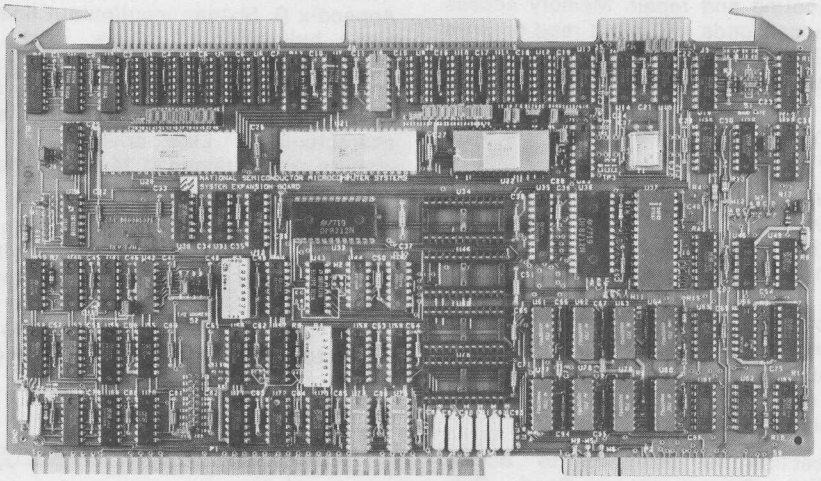
Note: For battery backup add -1 to part number (e.g., BLC-0512B-1).



BLC-0512B System Diagram

National Semiconductor

BLC-104 and BLC-116 Memory and Input/Output Boards



- **Flexible Memory Combinations**
  - 4K RAM and up to 8K PROM
  - 16K RAM and up to 8K PROM
  - 4K byte address boundaries
  - ROM can be implemented in 1K segments
- **Battery Back-Up Logic for System Memory Integrity**
- **48 Programmable Input/Output Lines for Digital Control Applications**
- **Synchronous/Asynchronous Serial Channel Permits Data Communication Interfacing to Data Set or Data Terminal with Baud Rates of 75 to 38.4K**
- **8 Maskable Interrupts and 1 millisecond Timer Permit Easy System Control**
- **Plug-replacements for SBC-104 and SBC-116**

Product Overview

The BLC-104 and BLC-116 Memory and Input/Output Expansion Boards provide a combination of memory and digital input/output capability ideally suited to smaller system applications where space and system optimization are critical.

Memory is provided for both read/write and read only requirements. The BLC-104 contains 4K bytes of dynamic RAM and sockets for up to 8K bytes of PROM while the BLC-116 contains 16K bytes of dynamic RAM and sockets for up to 8K bytes of PROM. ROM/PROM is implemented using MM2308/MM2316E ROM modules or MM2708/MM2716 PROM modules.

Both parallel and serial input/output are provided — 48 programmable parallel lines and one synchronous/asynchronous serial port. The 48 line programmable input/output capability may be configured to provide a variety of unidirectional and bidirectional combinations. The serial channel is capable of data transmission rates of up to 38.4K baud. Maskable interrupts and a one millisecond timer are included to provide complete system control.

The BLC-104 and BLC-116 are plug-replacements for Intel's SBC-104 and SBC-116 boards.

Functional Description

Read/Write Memory

The BLC-104 read/write RAM is based on National's MM4027 4K x 1-bit dynamic RAM modules; the BLC-116 uses MM4116 16K x 1-bit dynamic RAM modules. RAM modules are socket mounted for fast troubleshooting and repair. Memory access time is 575 nanoseconds and a full read or write cycle takes only 665 nanoseconds. Memory refresh is asynchronous and independent of the CPU. RAM addressing is switch selected, permitting its use on any 4K byte boundary within the 64K byte address range of the system.

Memory contents may be protected by using an auxiliary connector on the board. The logic connected to this line is TTL compatible and, when asserted as an active low from an external source, disables read and write access functions. This feature protects RAM contents during a system power-down sequence and permits the battery back-up to maintain the memory refresh function.

Read Only Memory

The ROM section is designed to accept MM2708/MM2716 Programmable Read Only Memory (PROM) or MM2308/MM2316E ROM modules. While four sockets are provided for the maximum configuration, only the number of PROM modules required for the application are necessary. ROM access time is a fast 465 nanoseconds with a maximum full cycle time of 685 nanoseconds.

The ROM section address is switch selected, permitting its use on any 4K byte boundary within the 64K byte address range of the system.

Parallel Input/Output

The 48 input/output lines are controlled by two INS8255 Programmable Peripheral Interface Circuits. Using standard Series/80 instructions, the 48 lines may be configured to a variety of 4 and 8 parallel line segments capable of latched or unlatched operation in bidirectional modes. The parallel input/output section is divided into six ports, each containing 8 bits.

Three basic modes of operation may be selected by program instructions:

- Data read or write to the specified port without the use of handshake signals. Output data is latched while input data is unlatched.
- Data read or write to the specified port using strobe or handshake signals created by or transmitted to the interfaced external device.
- Data read or write to the specified port using a bidirectional port to communicate with the external device. Handshake signals are provided by a separate "control" port (port 3 or 6).

Input/output modes for all ports are defined in Appendix B. Sixteen input/output lines have 8226 type bidirectional drivers and terminators permanently installed. The remaining 32 lines are fitted with sockets to permit user selection of drivers and terminators to match specific line characteristics. Line drivers and terminators circuits are contained in 14 pin DIP packages.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

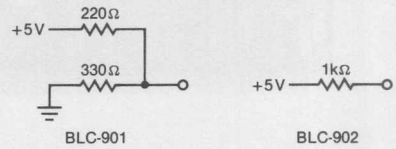


Figure 1. BLC-901 and BLC-902 Terminators

A variety of TTL compatible driver circuit types is available: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps (see Table I).

Table I. Drivers

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial Input/Output

The serial I/O port control is based on a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) circuit. The port is fully EIA RS232C compatible, thereby allowing interface with a wide range of data sets and data terminals. Standard Series/80 instructions control data transmission, and software is used to implement the desired transmission protocol technique. The port is double buffered for full duplex transmissions and

contains full data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and jumpers.

Synchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Automatic SYNC character insertion, 1 or 2 characters
- SYNC search
- External synchronization
- Even or odd parity

Asynchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Odd, even or no parity
- 1, 1½ or 2 stop bits
- False start bit detect
- Break character generation

Baud rate may be selected from the range 75 through 38.4K. Table II lists the rates available for synchronous and asynchronous data transmission. Three baud rates, based on a multiple of X1, X16 or X64 of the basic frequency, are program selectable.

Table II. Baud Rates

Synchronous	Asynchronous	
6980	75	1200
4800	110	2400
9600	150	4800
19200	300	9600
38400	600	19200

Error and status conditions are presented in the status word. Error condition may result from a framing error, data overrun (new character arrives before the buffer is empty) or incorrect parity. Figure 2 illustrates the status word.

The RS232C serial port may be converted to 20 ma current loop operation with an optionally available BLC-530 Current Loop Adapter. This permits interfacing devices such as teletypewriters, video displays and others not containing an RS232C compatible interface.

Interrupts

The BLC-104 and BLC-116 are designed to handle up to eight interrupt requests. Four may be jumper selected to permit automatic interrupt when a parallel character is received from or output to an external device.

Two interrupts may be configured to signal serial port character received and character transmitted.

The two remaining interrupt lines are shared by the 1 millisecond interval timer and two external event signal inputs.

The eight interrupts may be OR tied to form a single interrupt line to a system processor such as a BLC-80/10, or may be discrete when used with a system processor such as a BLC-80/204.

The eight interrupts may be individually masked under program control. The status of the interrupts is available to the system via the mask register.

I/O Section Addressing

The input/output section uses 16 contiguous addresses. The base, or board, address is jumper selectable to permit a high degree of system integration flexibility.

7	6	5	4	3	2	1	0
Data Set Ready	SYNC Detect	Framing Error	Data Overrun	Parity Error	Transmit Enable	Ready to Receive	Ready to Transmit

Figure 2. Status Word

BLC-116 — 16K bytes

Word Size — 8 bits

Access Time — 575 ns

Cycle Time — Read 665 ns
Write 665 ns
Refresh Delay 405 ns

Address Select — Switch and jumper selection
4K byte boundaries

ROM Memory

Memory Size — 8K bytes (PROM)

Word Size — 8 bits

Access Time — 465 ns

Address Select — Switch and jumper selection
4K byte boundaries

Parallel Input/Output

Number of Ports — 6

Number of Lines — 48

Configuration — Single, 4- or 8-bit

Data Transfer Modes — Unidirectional and bidirectional

Data Control — Latched, unlatched and strobed

Interface — TTL compatible

Compatible I/O Driver Modules —

Type	Output	Current (ma)
7400	I	16
7408	I, OC	16
7403	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting;
OC = open collector;
HV = high voltage)

Compatible I/O Termination Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial Input/Output

Control — Programmable USART

Transmission Modes — Synchronous and asynchronous

Parity — Odd, even or none

SYNC Functions — SYNC search
Automatic 1 or 2 SYNC character insertion

Asynchronous Stop Bits — 1, 1½ or 2

Asynchronous Break — Programmable control generation

Baud Rates — (asynchronous)

75	1200
110	2400
150	4800
300	9600
600	19200

External SYNC Control — Yes

Error Detection — Framing
Data overrun
Parity

Interface — RS232C

Interrupt — 8 lines
Program maskable
Discrete/OR tie capability

Timer — 1 millisecond intervals

System Bus Interface

All address, data and control signals are TRI-STATE™ TTL compatible.

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — 60 contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M "Schotchflex" 3463-001

Parallel I/O — 50 contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3415-001
AMP 2-86792-3
Recommended cables:
BLC-956 Parallel I/O Cable Kit
(two 5 foot ribbon cables)

Serial I/O	26 contact double-sided edge connector on 0.1-inch centers Recommended mating connector: 3M 3462-0001 flat AMP 1-583715-1 round

Power

	BLC-104	BLC-116	Battery
+5V	4.1 A	4.6 A	0.9 A
−5V	0.19 A	0.19 A	0.002 A
+12V	0.65 A	0.65 A	0.3 A
−12V	0.05 A	0.05 A	—

(Assumes ROM and I/O drivers installed.)

Environmental	Temperature 0° to 55 °C Humidity 0 to 90% non-condensing

Physical

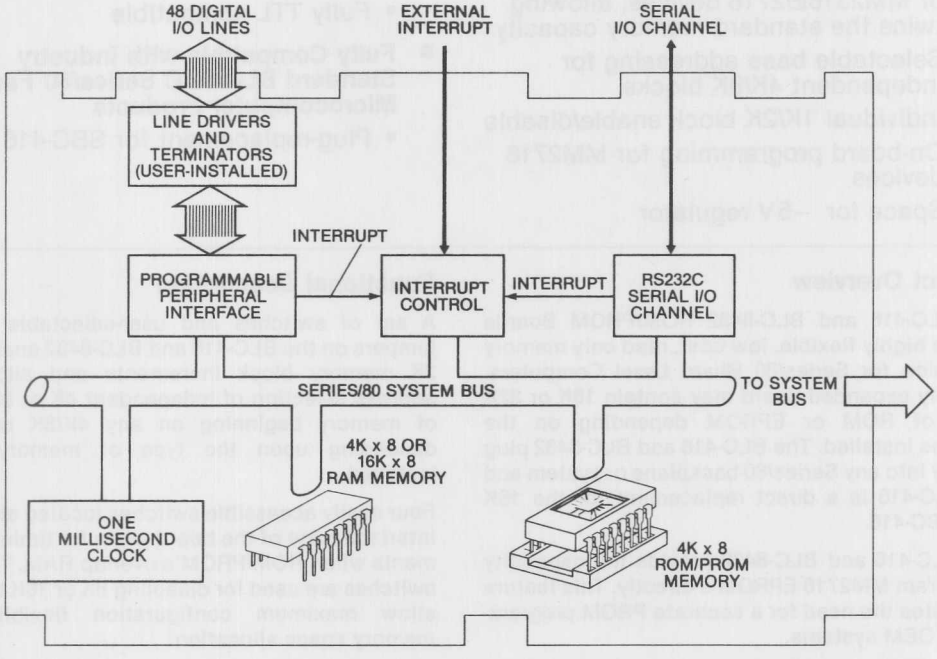
Height	6.75 in.	(17.15 cm)
Width	12.0 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

Order Information

BLC-104	RAM, ROM and I/O Expansion Board. Contains 4K bytes of dynamic RAM, sockets for 4K bytes of ROM or 8K bytes of PROM, 48 parallel and one serial I/O lines and 1 millisecond interval clock.
BLC-116	RAM, ROM and I/O Expansion Board. Contains 16K bytes of dynamic RAM, sockets for 4K bytes of ROM or 8K bytes of PROM, 48 parallel and one serial I/O lines, and a 1 millisecond interval clock.

Documentation

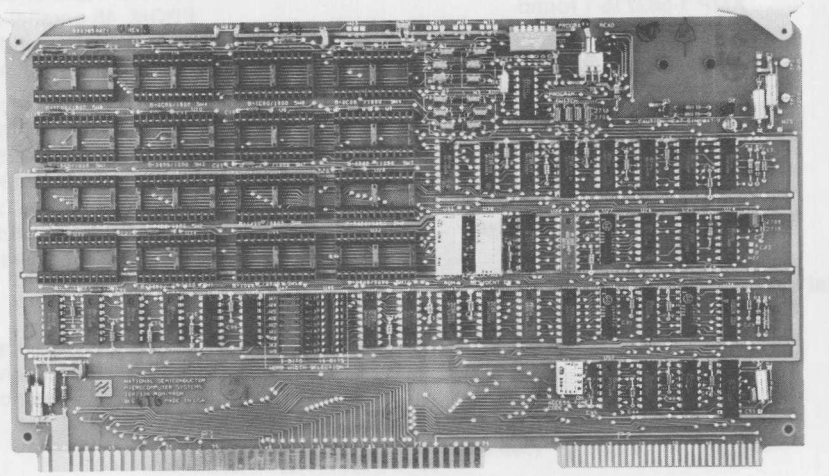
420305376-001	BLC-104/116/517 Input/Output and Memory Expansion Boards Hardware Reference Manual.



BLC-104 and BLC-116 Diagram

National Semiconductor

BLC-416 and BLC-8432
16K and 32K ROM/PROM Boards



- **Complete System Flexibility**
  - Jumper options select MM2308/2708 or MM2316E/2716 devices, allowing twice the standard memory capacity
  - Selectable base addressing for independent 4K/8K blocks
  - Individual 1K/2K block enable/disable
  - On-board programming for MM2716 devices
  - Space for −5V regulator
- **Ease of Use**
  - Buffered address and data lines
  - Fully TTL compatible
- **Fully Compatible with Industry Standard BLC/SBC Series/80 Family of Microcomputer Products**
  - Plug-replacement for SBC-416

Product Overview

The BLC-416 and BLC-8432 ROM/PROM Boards provide highly flexible, low cost, read only memory expansion for Series/80 Board Level Computers. The fully expanded board may contain 16K or 32K bytes of ROM or EPROM depending on the modules installed. The BLC-416 and BLC-8432 plug directly into any Series/80 backplane or system and the BLC-416 is a direct replacement for the 16K byte SBC-416.

The BLC-416 and BLC-8432 provide the capability to program MM2716 EPROM's directly. This feature eliminates the need for a separate PROM programmer in OEM systems.

To maintain compatibility with MDS systems not containing a −5V power bus, a low cost regulator may be installed on the board to provide −5V power to the PROM's.

Functional Description

A set of switches and user-selectable BERG™ jumpers on the BLC-416 and BLC-8432 enable 1K or 2K memory block increments and allow base address selection of independent 4K or 8K blocks of memory beginning on any 4K/8K boundary, depending upon the type of memory device installed.

Four easily accessible switches located at the user interface edge of the board allow for timing adjustments when ROM/PROM's overlap RAM. Two other switches are used for disabling 8K or 16K blocks to allow maximum configuration flexibility and memory space allocation.

Full interface and timing logic is provided to allow on-board programming of MM2716 devices. Where a programming voltage of +25VDC is applied through the auxiliary connector, the user can

program any device simply by issuing memory reference instructions from the system CPU. A status indicator and switch on the board display the mode of operation and thus prevent accidental programming.

Specifications

Memory Capacity —	BLC-416	16K bytes in 1K increments
	BLC-8432	32K bytes in 2K increments
Word Size —	8 bits (16-bit jumper selected option)	
Compatible Memory Devices —	MM2308 ROM MM2708 EPROM MM2316E ROM MM2716 EPROM	
Address Selection —	2308/2708 devices — 4K banks on 4K boundaries 2316E/2716 devices — 8K banks on 8K boundaries	
System Bus Interface —	Address, control, and data lines are TRI-STATE™ TTL compatible	
Connectors —		
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers	
Auxiliary	60 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: AMP P35-14559 TI H311130	

Power —	VDC	Fully loaded 2708 EPROM's	Fully loaded 2716 EPROM's
	+5V	0.01 A	1.40 A
	−5V	0.72 A	—
	+12V	1.04 A	—
	−12V	—	—
	−25V ± 1V (Programming Voltage)	—	0.12 A

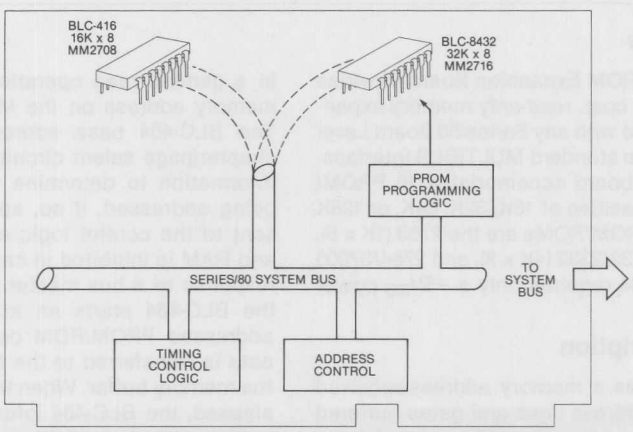
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-416	ROM/PROM Expansion Board factory configured for 2308/2708 devices. Sockets provide a total of 16K bytes of memory.
BLC-8432	ROM/PROM Expansion Board factory configured for 2316E/2716 devices. Sockets provide a total of 32K bytes of memory.

Documentation

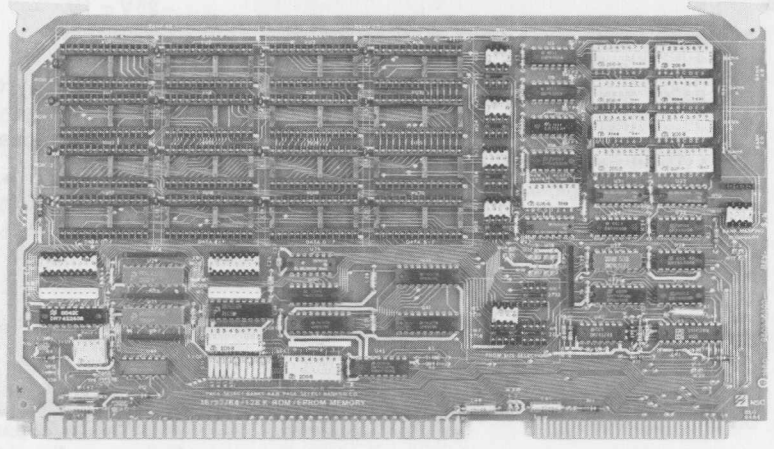
420305447-001	BLC-416/8432 16K/32K ROM/PROM Board User's Manual



BLC-416 and BLC-8432 Diagram

National Semiconductor

BLC-464
128K PROM/ROM Expansion Board



- **16K to 128K Capacity Compatible With Seven PROM (ROM) Device Types: 2758, 2716 (2316), 2732 (2332), or 2764 (37000)**
- **Single 5V Power Supply**
- **Plugs Into Standard BLC-604/614 Card Cage or Equivalent**
- **Compatible With Industry Standard MULTIBUS™ (IEEE 796)**
- **Address-Assignable Anywhere Within 16M Byte Memory**
- **Switch-Selectable Minimum Access Time From 35 ns to 1435 ns**
- **Operation in 8-Bit or 16-/8-Bit Mode**
- **Plug Replacement for SBC-464, With Doubled Capacity**

Product Overview

The BLC-464 PROM/ROM Expansion Board provides a highly flexible, low cost, read-only memory expansion board compatible with any Series/80 Board Level Computer through the standard MULTIBUS interface. The fully expanded board accomodates 16 PROM/ROM devices for capacities of 16K, 32K, 64K, or 128K bytes. Compatible PROM/ROMs are the 2758 (1K x 8), 2716/2316 (2K x 8), 2732/2332 (4K x 8), and 2764/37000 (8K x 8). The BLC-464 requires only a $+5V_{DC}$ power supply.

Functional Description

The BLC-464 decodes a memory address received on the MULTIBUS address lines and gates buffered memory data back to the bus. The user selects memory size, memory organization, base addresses, and board access time with on-board DIP switches, option blocks, and Berg jumpers.

In a general read operation, a bus master puts a memory address on the MULTIBUS address lines. The BLC-464 base address select circuitry and chapter/page select circuitry decode the incoming information to determine whether the BLC-464 is being addressed. If so, appropriate information is sent to the control logic and chip select circuitry, and RAM is inhibited in case of address overlap. In response to a bus master memory read command, the BLC-464 starts an access time counter, the addressed PROM/ROM devices are selected, and data is transferred to the MULTIBUS data lines via the memory buffer. When the board access time has elapsed, the BLC-464 informs the bus master that memory data is available on the bus. The bus master then accepts the data and issues a signal ending the read operation.

MULTIBUS is a trademark of Intel Corp.

The BLC-464 meets the specifications for a MULTIBUS™ slave module. It is compatible with systems using up to 24 address lines and accommodates both 8-bit and 16-bit data paths.

The memory array consists of four banks and four rows of PROM/ROM devices for a total of sixteen. Data sent to the memory buffer during a read operation may be gated out as a 16-bit word or multiplexed onto the low order bus data lines as high order and low order 8-bit bytes. The latter is used when 16-bit words are being treated by an 8-bit microprocessor. The PROM/ROM device memory size and selected bit mode determine the array addressing structure.

The control logic circuitry receives signals from the base address select circuit and the MULTIBUS interface and controls the general operation of the board. These control functions include disabling the board for RAM access when address overlap (PROM/ROM and RAM sharing common addresses) is used, synchronizing board access time, and establishing correct address in-data out protocol with the bus.

While 64K bytes of PROM/ROM may be addressed directly, larger systems require the use of a chapter/page division of memory. In this format, 16 chapters, each containing sixteen 64K byte pages, are available. Chapter and page addresses on the BLC-464 are set by on-board DIP switches. These allow the BLC-464 memory to be assigned anywhere within the 16M bytes of available space. The chapter/page select circuitry determines whether the extended address lines are addressing memory. Any area of RAM overlap is also established by on-board DIP switches. When RAM in the overlapping area is addressed, BLC-464 access time is increased to 1435 ns (minimum) to allow the RAM access cycle to be completed.

Specifications

Memory Capacity —	16K, 32K, 64K, or 128K bytes
Word Size —	8-bit or 16-8-bit
Compatible Memory Devices —	2758 PROM (1K x 8 = 16K) 2716 PROM (2K x 8 = 32K) 2316 ROM 2732 PROM (4K x 8 = 64K) 2332 ROM 2764 PROM (8K x 8 = 128K) 37000 ROM
Address Selection —	Divided into 16 chapters of 16-64K pages; assignable anywhere within 16M byte memory space
System Bus Interface —	MULTIBUS™ system compatible

Connectors

System Bus	86-contact double-sided card cage edge connector on 0.156 inch centers
Auxiliary	60-contact double-sided edge connector on 0.1 inch centers Recommended mating connectors: AMP P35-14559 TI H311130

Power $V_{CC} = +5V_{DC} \pm 5\%$

PROM/ ROM Used	Memory Size	Current
2758	16K	2.25A
2716	32K	2.25A
2316E	32K	3.00A
2732	64K	2.49A
2332	64K	2.00A
2764	128K	2.70A
37000	128K	1.90A

Environmental
Temperature 0°C to −55°C
Humidity 0-90% non-condensing

Physical

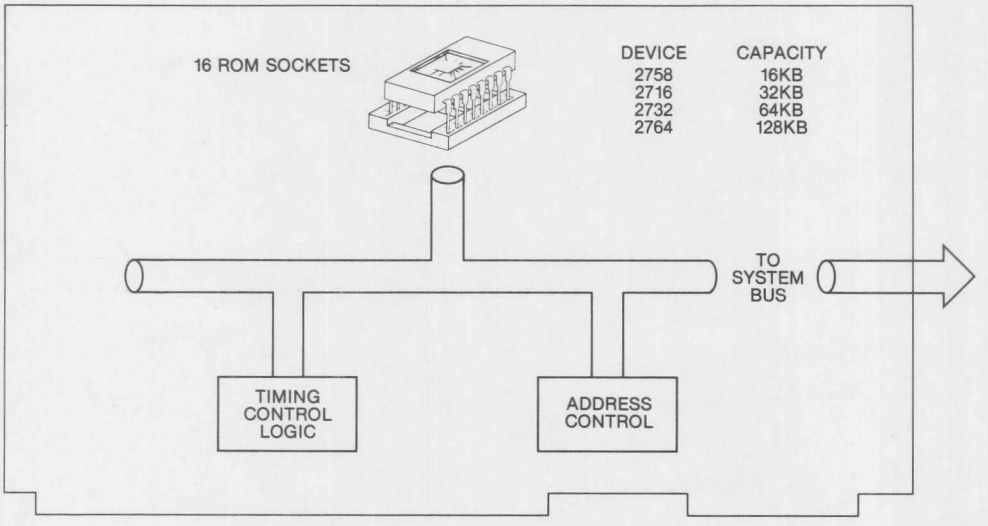
Height	6.75 in. (17.15 cm)
Width	12.00 in. (30.48 cm)
Depth	0.50 in. (1.27 cm)
Weight (w/o PROM/ROMS)	10.5 oz. (295 gm)

Order Information

BLC-464	16K/32K/64K/128K PROM/ROM Expansion Board Sixteen sockets provide memory capacity according to user's selection of PROM/ROM devices.

Documentation

420306303-001	BLC-464 PROM/ROM Expansion Board Hardware Reference Manual

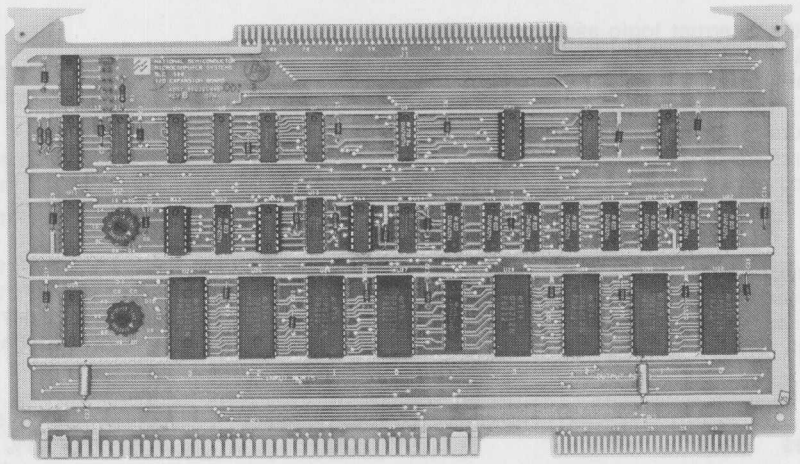


BLC-464 Block Diagram

Section 5
I/O Expansion Boards

National Semiconductor

BLC-508
Input/Output Expansion Board



- **Independently Controlled 8-bit Parallel Ports**
  - Four input ports
  - Four output ports
- **Variable Width Strobed Outputs Permit Synchronization with External Devices**
- **Interrupts for Reduced System Overhead Control**
  - Automatic input port interrupt
  - Eight external available
- **Switch Selected Port Address for System Integration Flexibility**
- **Plug-replacement for SBC-508**

Product Overview

The BLC-508 Input/Output Expansion Board is specifically designed as an economical solution for limited digital input/output application requirements where system computer input/output line capacity is exhausted.

The BLC-508 provides four 8-bit input ports and four 8-bit output ports, each individually addressable. Input and output operation is governed by an on-board strobe with a variable interval to meet a variety of external timing requirements.

The BLC-508 is a plug-replacement for Intel's SBC-508 board.

Functional Description

Input

The input section contains four independent 8-bit ports. Incoming data is latched or unlatched in the input buffer. A buffer full interrupt may be generated to the system CPU to signal data availability.

TRI-STATE™ TTL compatible 8212 devices permit interfacing to a wide range of external devices. Input lines are terminated with 1K ohm pull-up resistors contained in 14-pin DIP modules and mounted in on-board sockets.

Output

The output section contains four independent 8-bit ports. Data is presented to the output port using an I/O write command from the system CPU. Output data is latched in the output buffer. The output strobe to the external device signals the device that data is available.

TRI-STATE™ TTL compatible 8212 devices are used to permit interfacing to a wide range of external devices. Each output line is capable of driving a 48 milliamp load.

The output strobe is variable to permit synchronization with the peripheral device requirements. The strobe pulse width may be jumper selected to 100, 200, 400, 800 or 1600 nanoseconds.

Interrupts

In addition to the interrupt logic associated with the input ports, the BLC-508 contains 8 line external interrupt control. The interrupt driven I/O control feature may be implemented in one of two ways: as a discrete interrupt level or as a single level multi-sourced interrupt. Interrupts are automatically cleared after servicing.

Addressing

Input and output ports use eight contiguous addresses. The base address is the lowest of the eight and is selected by on-board switches. This permits a high degree of system integration flexibility.

Specifications

Number of Input Ports —	4
Number of Output Ports —	4
I/O Port Data Width —	8-bit
I/O Buffer Mode —	Latched
Input Termination —	1K ohm
Output Drive —	48 ma
Output Strobe Width —	Variable 100, 200, 400, 800 or 1600 ns
External Interrupt Capacity —	8
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible.
Connectors	
System Bus	86 contact double-sided card cage edge connector on 0.156 inch centers
Input/Output	100 contact double-sided edge connector on 0.1 inch centers Recommended mating connector: Arco AE150WP11 AE150WP21 Eko 006307100472001 CDC VPB01B50A00A1
Power —	+5V, 2.2 A
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing

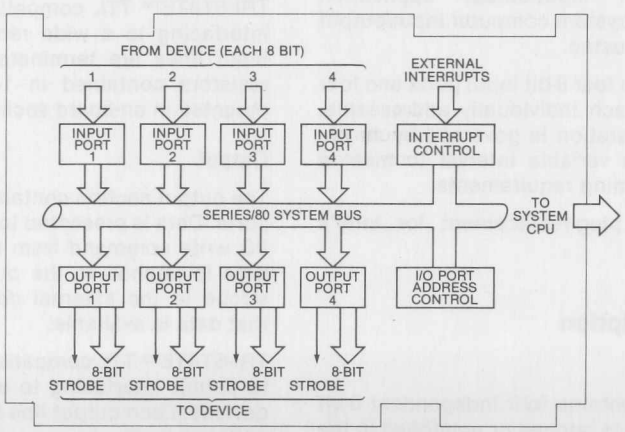
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-508	Input/Output Expansion Board. Contains 8 independent input and output 8-bit parallel ports.

Documentation

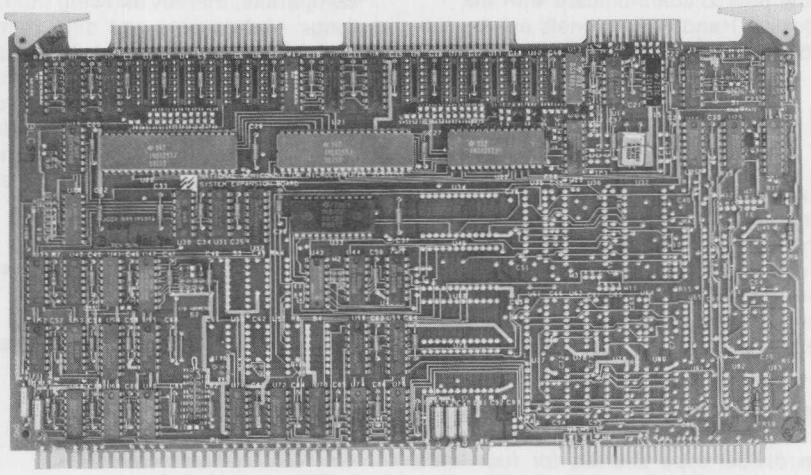
420305448-001	BLC-508 Input/Output Board Hardware Reference Manual



BLC-508 Diagram

National Semiconductor

BLC-517
Input/Output Expansion Board



- **48 Programmable Input/Output Lines for Digital Control Applications**
- **Synchronous/Asynchronous Serial Channel Permits Data Communication Interfacing to Data Set or Data Terminal**
- **Baud Rates of 75 to 38.4K Allow Interfacing to Broad Range of Serial Input/Output Devices**
- **8 Maskable Interrupts for Easy System Control**
- **1 Millisecond Interval Timer for Automatic Time Controlled Sequences**
- **Compatible with BLC/SBC Series/80 Software and Hardware**
- **Plug-replacement for SBC-517**

Product Overview

The BLC-517 Combination Input/Output Expansion Board complements the broad range of BLC/SBC Series/80 Board Level Computers with digital input/output expansion capability.

Both parallel and serial input/output are provided: 48 programmable parallel lines and one synchronous/asynchronous serial port. The 48 line programmable input/output capability may be configured to provide a variety of unidirectional and bidirectional combinations. The serial channel is capable of data transmission rates of up to 38.4K baud. Maskable interrupts and a one millisecond timer are included to provide complete system control.

The BLC-517 is a plug-replacement for Intel's SBC-517.

Functional Description

Parallel Input/Output

The 48 input/output lines are controlled by two INS8255 Programmable Peripheral Interface Circuits. Using standard Series/80 instructions, the 48 lines may be configured to a variety of 4 and 8 parallel line segments capable of latched or unlatched operation in unidirectional and bidirectional modes. The parallel input/output is divided into six ports, each containing 8 bits.

Three basic modes of operation may be selected by program instructions:

- Data read or write to the specified port without the use of handshake signals. Output data is latched while input data is unlatched.

- Data read or write to the specified port using a bidirectional port to communicate with the external device. Handshake signals are provided by a separate "control" port (port 3 or 6).

Input/output modes for all ports are defined in Appendix B.

Sixteen input/output lines have 8226 type bidirectional drivers and terminators permanently installed. The remaining 32 lines are fitted with sockets to permit user selection of drivers and terminators to match specific line characteristics. Line driver and terminator circuits are contained in 14 pin DIP packages.

National's BLC-901 and BLC-902 terminator modules are available as options to satisfy termination requirements. The BLC-901 contains 220/330 ohm divider type circuits for four lines, while the BLC-902 contains 1K ohm pull-up type terminator circuits for four lines. Figure 1 illustrates the terminator circuit configuration.

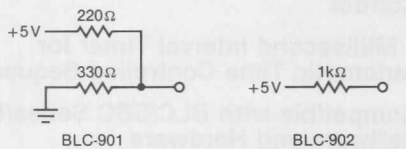


Figure 1. BLC-901 and BLC-902 Terminators

A variety of TTL compatible driver circuit types is available: inverting, non-inverting, high voltage and open collector combinations with sink current capacity ranging from 16 to 48 milliamps. (See Table I.)

Table I. Drivers

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Synchronous/Asynchronous Receiver/Transmitter (USART) circuit. The port is fully EIA RS232C compatible, thereby allowing interface with a wide range of data sets and data terminals. Standard Series/80 instructions control data transmission, and software is used to implement the desired transmission protocol technique. The port is double buffered for full duplex transmissions and contains full data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and jumpers.

Synchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Automatic SYNC character insertion, 1 or 2 characters
- SYNC search
- External synchronization
- Even or odd parity

Asynchronous transmission features:

- 5-, 6-, 7- or 8-bit characters
- Odd, even or no parity
- 1, 1½ or 2 stop bits
- False start bit detect
- Break character generation

Baud rate may be selected from the range 75 through 38.4K. Table II lists the rates available for synchronous and asynchronous data transmission. Three baud rates, based on a multiple of X1, X16 or X64 of the basic frequency, are program selectable.

Table II. Baud Rates

Synchronous	Asynchronous	
6980	75	1200
4800	110	2400
9600	150	4200
19200	300	9600
38400	600	19200

Error and status conditions are presented in the status word. Error condition may result from a framing error, data overrun (new character arrives before the buffer is empty) or incorrect data parity. Figure 2 illustrates the status word.

7	6	5	4	3	2	1	0
Data Set Ready	Sync Detect	Framing Error	Data Overrun	Parity Error	Transmit Enable	Ready to Receive	Ready to Transmit

Figure 2. Status Word

The RS232C serial port may be converted to 20 ma current loop operation with an optionally available BLC-530 Current Loop Adapter. This permits interfacing devices such as teletypewriters, video displays and others not containing an RS232C compatible interface.

Interrupts

The BLC-517 is designed to handle up to eight interrupt requests. Four may be jumper selected to permit automatic interrupt when a parallel character is received from or output to an external device.

Two interrupts may be configured to signal serial port character received and character transmitted.

The two remaining interrupt lines are shared by the 1 millisecond interval timer and two external event signal inputs.

The eight interrupts may be OR tied to form a single interrupt line to a system processor such as a BLC-80/10, or may be discrete when used with a system processor such as a BLC-80/204.

The eight interrupts may be individually masked under program control. The status of the interrupts is available to the system via the mask register.

Addressing

The BLC-517 uses 16 contiguous addresses. The base, or board, address is jumper selectable to permit a high degree of system integration flexibility.

Specifications

Parallel Input/Output

Number of Ports — 6

Number of Lines — 48

Configuration — Single, 4- or 8-bit

Data Transfer Modes — Unidirectional and bidirectional

Data Control — Latched, unlatched and strobed

Interface — TTL compatible

Compatible I/O Driver Modules —

Type	Output	Current (ma)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Compatible I/O Termination Modules — BLC-901 220/330 ohm divider
BLC-902 1K ohm pull-up

Serial Input/Output

Control — Programmable USART

Transmission Modes — Synchronous and asynchronous

Character Length — 5-, 6-, 7- or 8-bit

Parity — Odd, even or none

SYNC Functions — SYNC search
Automatic 1 or 2 SYNC character insertion

Asynchronous Stop Bits — 1, 1½ or 2

Asynchronous Break — Programmable control generation

Baud Rates — (asynchronous)

75	1200
110	2400
150	4800
300	9600
600	19200

External SYNC Control — Yes

Error Detection — Framing
Data overrun
Parity

Interface — RS232C

Interrupt — 8 lines
Program maskable
Discrete/OR tie capability

Timer 1 millisecond intervals

System Bus Interface

All address, data and control signals are TRI-STATE™ TTL compatible.

Connectors

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Auxiliary — 60 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559
TI H311130

Parallel I/O — 50 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3415-001
AMP 2-86792-3

Recommended cables:
BLC-956 Parallel I/O Cable Kit
(two 5 foot ribbon cables)

Serial I/O 26 contact double-sided edge connector on 0.1 inch centers

Recommended mating connector:
3M 3462-0001 flat
AMP 1-583715-1 round

Power +5V, 2.4 A
+12V, 0.04 A
−12V, 0.06 A

Environmental Temperature 0° to 55°C
Humidity 0 to 90%
non-condensing

Physical

Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 g)

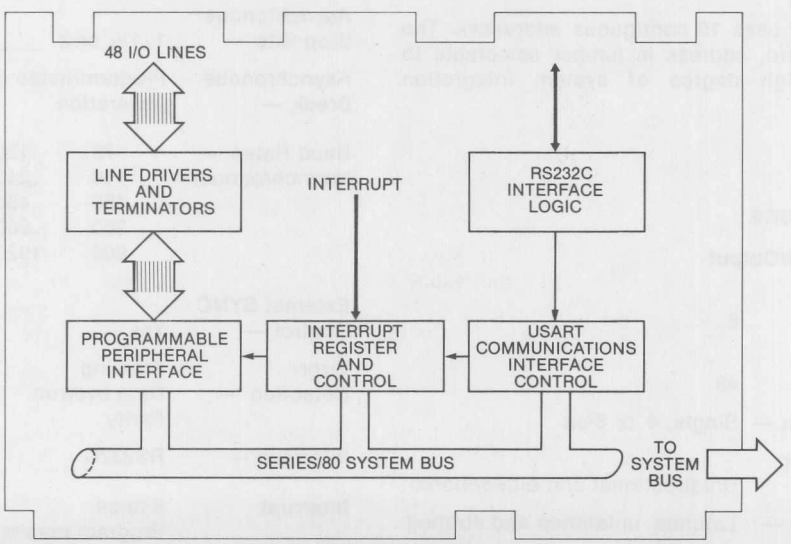
Order Information

BLC-517 Input/Output Expansion Board
Contains 48 parallel and one serial programmable I/O lines, interrupt capability and 1 millisecond interval timer.

BLC-956 Parallel I/O Cable Kit
Contains two 5 foot ribbon cables for connection to parallel input/output board edge connectors.

Documentation

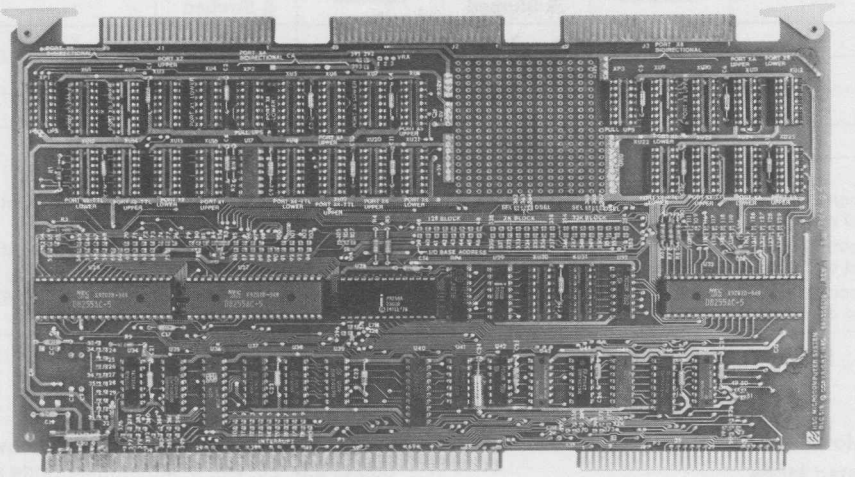
420305376-001 BLC-104/116/517 Input/Output and Memory Expansion Boards Hardware Reference Manual



BLC-517 Diagram

National Semiconductor

BLC-519
Programmable I/O Expansion Board



- **72 Programmable I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **I/O or Memory-Mapped Using 8 or 16 Address Lines**
- **Interval Timer with Jumper Selectable Frequencies (0.5, 1.0, 2.0, or 4.0 ms, or User-Defined**
- **Eight Levels of Maskable Interrupts, Expandable to 64**
- **Prototyping Area with All Supply Voltages Available**
- **Plug Replacement for SBC-519**
- **Compatible with all Series/80 Boards and Card Cages**

Product Overview

The BLC-519 Programmable I/O Expansion Board is specifically designed for digital I/O intensive computer systems. It provides 72 additional I/O lines for any Series/80-Multibus™ compatible system.

Not only are extra lines provided, but facilities for conveniently using them are present. Eight levels of interrupts are implemented with a programmable interrupt controller. These can be expanded to 64 levels if desired. An interval timer allows the use of commonly used frequencies, as well as the ability to define unique values via the P2 auxiliary connector. Not only can the BLC-519 be I/O-mapped as is done in many systems today, but can also be memory-mapped. Either method can be configured to use 8 or 16 address lines. A prototyping area is provided for user-defined, unique capabilities not required by all computer systems.

The BLC-519 is strapped for shipment to be a plug-replacement for Intel's SBC-519.

Multibus is a trademark of Intel Corp.

Functional Description

Input/Output

The BLC-519's 72 programmable I/O lines are implemented with three 8255A's. They can be operated in any of their three modes: basic input/output, strobed input/output, and bidirectional bus (see Table 1). Each is connected to its own 50-pin card edge connector through sockets in which the user can plug line drivers or terminators to "customize" the interface. Each 8255A has two interrupt sources which may be jumpered into the programmable interrupt controller, or directly to the Multibus.

Programmable Interrupt Controller

An 8259A provides the programmable interrupt control for the BLC-519. It resolves priority among the interrupt inputs according to a program-selected algorithm. A variety of algorithms are available to the user so that interrupt handling can be adapted to different system characteristics:

						Bidirectional	Control
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1,4,7	8	X	X	X	X	X	
2,5,8	8	X	X	X	X		
3,6,9	4	X		X			X[1,2,3]
	4	X		X			X[1,2,3]

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.
3. Part of port 9 must be used as a control port when either port 7 or port 8 are used as a latched and strobed input or a latched and strobed output port or port 7 is used as a bidirectional port.

- Nested Mode
- Fully Nested Mode
- Automatic Rotating Mode
- Specific Rotating Mode
- Slave (Bus Vectored and Non-Bus Vectored) Mode
- Special Mask Mode
- Polled Mode

The user has the option of bypassing the 8259A and driving the Multibus interrupt lines directly.

The BLC-519 also features a cascadeable PIC arrangement. This permits it to be used in a system of one "master" and up to eight "slaves". A master is defined by a jumper on one of the BLC-519's, whereas the rest must be slaves. When a slave request line is activated, and subsequently acknowledged, the master will enable the corresponding BLC-519 slave to release the interrupt vector. This allows for expansion of up to 64 interrupt levels.

Interrupt Sources

There are ten interrupt sources on the BLC-519: six from the 8255A's, three from external devices (one through each I/O card edge connector), and one from the interval timer. A jumper matrix allows the selection of any eight of these for input to the programmable interrupt controller. The PIC then translates these into a single Multibus interrupt request. (The eight selected lines can be jumped to drive the Multibus interrupt request lines directly.)

Interval Timer

A user-selectable interval timer is provided. If periods of 0.5, 1.0, 2.0, or 4.0 milliseconds are appropriate for the application, then placement of a jumper is all that is required. If different intervals are preferred, a user-defined signal can be applied to pin 46 of the P2 auxiliary connector. Periods of 0.5X, 1X, 2X, or 4X can now be used via jumper placement. of the P2 auxillary connector. Periods of 0.5X, 1X, 2X, or 4X can now be used via jumper placement.

Multibus Interface

The BLC-519 is shipped as an I/O mapped slave with 8-bit base address decoding on 16 address boundaries. With the addition of user-installed 3205/8205's, address decoding can be extended to 16 bits. This provides 4096 possible base addresses, allowing more flexibility in 16-bit systems.

An additional convenience inherent in the BLC-519 is that it can be configured to be a memory-mapped board. In 8-bit systems which are I/O intensive, this ensures that the user will not run out of I/O addressability.

The advanced acknowledge (AACK/) and transfer acknowledge (XACK/) signals are adjustable to obtain maximum throughput in any Series/80-Multibus computer system.

Prototyping Area

A prototyping area is provided on the BLC-519 for the user. Circuitry for I/O voltage level translation or for conversion from BCD to 7-segment for displays are potential uses. Sources of $\pm 5\,V_{DC}$ and $\pm 12\,V_{DC}$ are near this area, as are provisions for bypass capacitors for these voltages.

Specifications

Addressing

Base Address= $XYZO_{HEX}$ (See Note 1)

where: —X and Y = 0 as shipped (8-bit address decode), and Z is any hexadecimal digit
—X, Y, and Z = any hexadecimal digit when additional 3205/8205's are installed by user

Address	Device	Function
BASE + 0	8255A No. 1	Port 1 (Port A)
BASE + 1	8255A No. 1	Port 2 (Port B)
BASE + 2	8255A No. 1	Port 3 (Port C)
BASE + 3	8255A No. 1	Control
BASE + 4	8255A No. 2	Port 4 (Port A)
BASE + 5	8255A No. 2	Port 5 (Port B)
BASE + 6	8255A No. 2	Port 6 (Port C)
BASE + 7	8255A No. 2	Control
BASE + 8	8255A No. 3	Port 7 (Port A)
BASE + 9	8255A No. 3	Port 8 (Port B)
BASE + A	8255A No. 3	Port 9 (Port C)
BASE + B	8255A No. 3	Control
BASE + C	8259A	In-Service Register
BASE + C	8259A	Command Register
BASE + C	8259A	Status (Polling Register)
BASE + D	8259A	Interrupt Request Register
BASE + D	8259A	Mask Register
BASE + D	8259A	Block Address Register
BASE + E	Interval Timer	Read or Clear
BASE + F	Interval Timer	Read or Clear

Notes: 1. May be memory-mapped or I/O mapped.
2. Several 8259A registers have the same address, so sequence of access and control word determine which register responds.

Interrupt Sources — 6-8255A's 3-External sources (through I/O conectors)
1-Interval timer

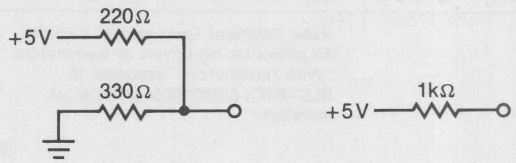
Interval Timer — A user-selectable interval timer is provided. If periods of 0.5, 1.0, 2.0, or 4.0 milliseconds are appropriate for the applica tion, then placement of a jumper is all that is required. If different intervals are preferred, a user-defined signal can be applied to pin 46 of the P2 auxiliary con nector. Periods of 0.5X, 1X, 2X, or 4X can now be used via jumper placement.

Line Drivers and Terminators — I/O Drivers: The following line drivers are compatible with all I/O sockets.

Driver	Characteristic	Sink Current (mA)
7400	I	16
7403	I,OC	16
7408	NI	16
7409	NI,OC	16
7426	I,OC	16
7432	NF	16
7437	I	48
7438	I,OC	48

Note: I = inverting, NI = non-inverting, OC = open collector

I/O Terminators — The following terminators are compatible with all I/O sockets.



BLC-901 BLC-902

Ports 1, 4, and 7 may use any of the drivers or terminators shown above for unidirectional (input or output) port configurations. Either terminator and the following bidirectional drivers and terminators may be used for ports 1, 4, and 7 when these ports are used as bidirectional ports.

Bidirectional Drivers

Driver	Characteristic	Sink Current (mA)
8216	NI,TS	25
8226	I,TS	50

Note: I = inverting, NI = non-inverting, TS = tri-state

Terminators

Supplier	Product Series
CTS Dale Beckman	.760- LDP14k-02 899-1

Connectors

System Bus — 86 contact, double-sided card edge connector on 0.156 inch centers

Recommended Connectors:

CDC	VPB01E43A00A1
Viking	2V43/1 and 5

Auxiliary Bus — 60 contact, double-sided card edge connector on 0.1 inch centers

Recommended Connectors

AMP	PE5-14559
TI	H311130

Parallel I/O — 50 contact, double-sided card edge connector on 0.1 inch centers

Recommended Connectors

3M	3415-000
TI	H312125

Power

Voltage	Without Terminators	With Terminators
$V_{CC} = +5V \pm 5\%$	$I_{CC} = 1.2A$ Max.	$I_{CC} = 3.1A$ Max.

Note: "Without Terminators" includes no power for I/O drivers or terminators. "With Terminators" assumes 18 BLC-901's (220Ω/330Ω terminator) installed.

Environmental

Temperature — 0°C to 50°C

Humidity — 0% to 90% non-condensing

Physical

Height — 6.75 in. (17.15 cm)

Width — 12.00 in. (30.48 cm)

Depth — 0.50 in. (1.27 cm)

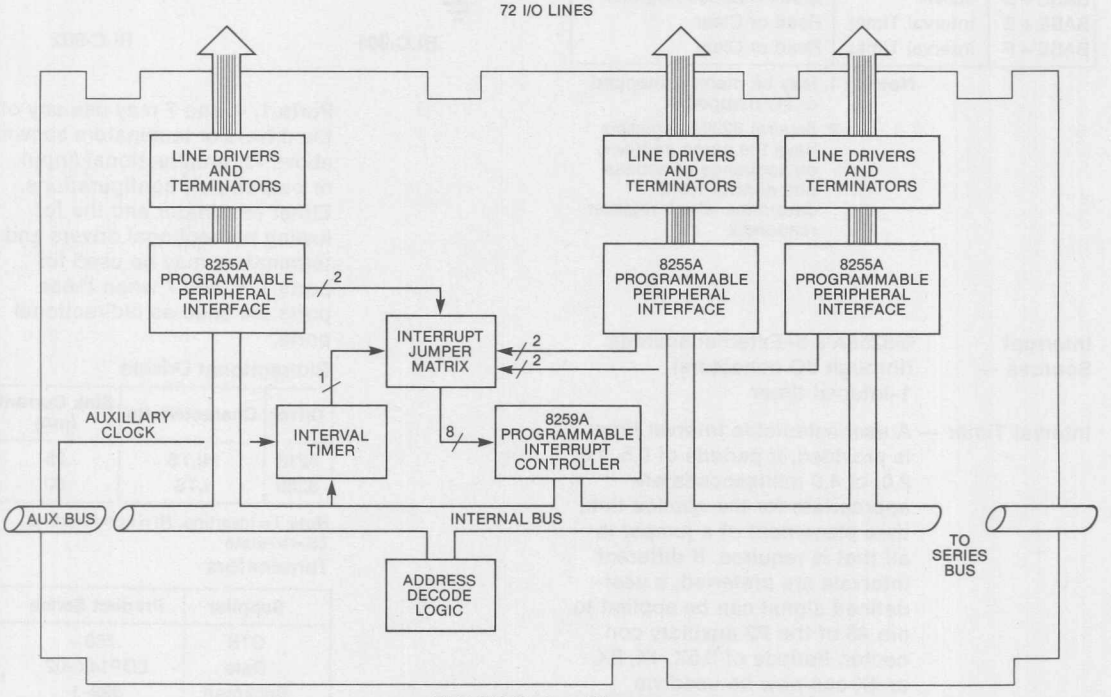
Weight — 14 oz. (396.9 gm)

Order Information

BLC-519 — Programmable I/O Expansion Board. Includes 72 digital I/O lines, programmable interrupt controller, and an interval timer.

Documentation

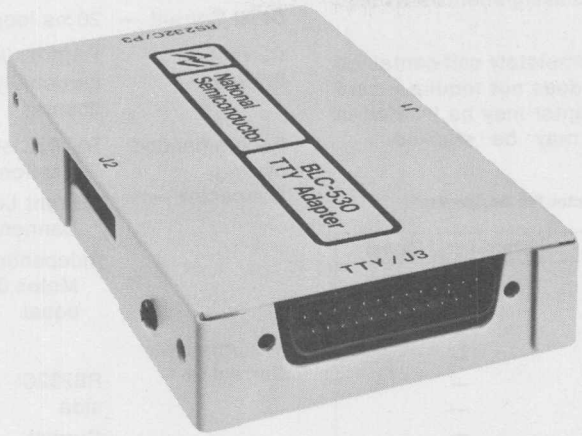
42030 -001 — BLC-519 Hardware Reference Manual



BLC-519 System Diagram

National Semiconductor

BLC-530
Current Loop Adapter



- **Current Loop Conversion for RS232C Serial I/O Channels Extends Series/80 Capability**
- **Data Set or Data Terminal Configuration for Application Flexibility**
- **Fully Compatible with BLC/SBC CPU's and I/O Expansion Boards**
- **Plug-replacement for SBC-530**

Product Overview

National's BLC-530 Current Loop Adapter provides an ideal low cost solution for converting an RS232C serial input-output channel to a 20 milliamperes current loop mode.

Designed in anticipation of the need for application flexibility, the BLC-530 may be used with Series/80 microcomputer and I/O boards when connection is made between the computer and a current loop device, between the computer and a data set, or between a data set and a current loop device.

The BLC-530 easily accommodates a wide variety of applications. It is housed in a small independent container and, thus, does not occupy valuable board slots. This can result in savings in system space and cost.

Fully plug-compatible with Intel's SBC-530, the National BLC-530 may be used with any Intel, National or equivalent Series/80 system.

Functional Description

The BLC-530 Current Loop Adapter is a passive device capable of responding to full or half duplex transmissions without reconfiguration. The line interface on the current loop side of the adapter is optically coupled to assure current loop and RS232C signal isolation.

Current for the current loop is derived from one of two sources. In the standard configuration the adapter derives power from the RS232C serial input-output port 12 volt source. Optionally, the user may reconfigure the adapter to allow power to be supplied from an independent source. A Molex connector is incorporated as an integral part of the adapter for this purpose. Configurations are simply and easily changed by repositioning BERG™ jumpers — no tools or wire are necessary.

The adapter contains two 25-pin connectors for interconnecting the RS232C and current loop channel. Inadvertent cable cross connection is prevented by using a socket-type connector for the RS232C side and a plug connector for the current

cable. The RS232C cable connector mates to the BLC-530 and to a Series/80 board serial I/O port edge connection. Pin signal assignments are listed in Table I.

Because the BLC-530 is completely self-contained in a separate container it does not require a card cage slot. Instead, the adapter may be located in any desired place and may be stacked.

Table I. BLC-530 Connector Pin Assignments

Pin	RS232C Signal	Current Loop Signal
1	Ground	Ground
2	Transmit Data	—
3	Receive Data	—
4	Request to Send	—
5	Clear to Send	—
6	Data Set Ready	—
7	Ground Carrier Detect	—
11	+12V	—
12	—	TTY Receive
13	Sec Clear to Send	TTY Transmit
14	Sec Transmit Data	—
15	Transmit Clock	—
16	Sec Receive Data	TTY Read Control
17	Receive Clock	—
19	Sec Request to Send	—
20	Data Terminal Ready	—
21	—	TTY Read Control Return
22	Ring Indicator	—
23	−12V	—
24	DTE Transmit Clock	TTY Receive Return
25	—	TTY Transmit Return

Interface Standard — EIA RS232C

Drive Current — 20 ma loop

Current Source — RS232C I/O Port (optionally from independent source)

Recommended Mating Connector —
RS232C side:
Cannon DB-25S or equal
Current Loop Side:
Cannon DB-25P or equal
Independent Power:
Molex 09-50-7071 with pins or equal

Maximum Current —

	+12V	−12V
RS232C side	30 ma	30 ma
Current Loop side	40 ma	40 ma

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —

Height	4.85 in.	(12.32 cm)
Width	2.88 in.	(7.31 cm)
Depth	0.92 in.	(2.34 cm)
Weight	9 oz.	(255.2 g)

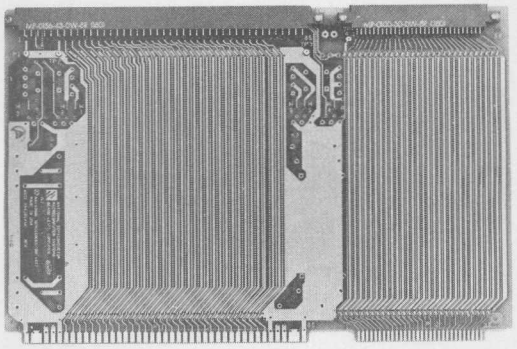
Order Information

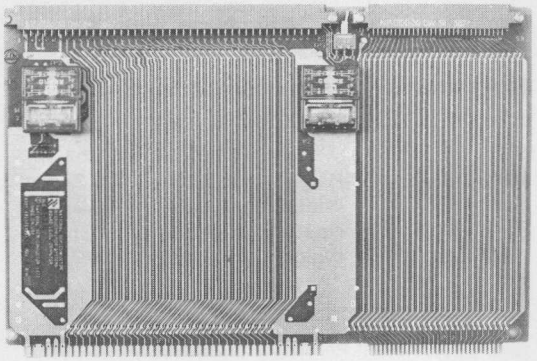
BLC-530 Current Loop Adapter

BLC-955 I/O Cable Kit
Consists of one 5 foot RS232C serial I/O cable and one 2.5 foot current loop cable.

National Semiconductor

BLC-610 and BLC-8610 Extender Boards





- **Power Isolation in BLC-8610 Allows Removal/Insertion of Boards without Loss of Data or Functions**
- **Easily Accessible Test Points for Fast Bus and Control Signal Examination**
- **Complete Access to a Series/80 Board for Troubleshooting or Debugging**
- **BLC-610 is Plug-replacement for Intel's MDS-610**

Product Overview

The BLC-610 and BLC-8610 Extender Boards may be used to extend Series/80 family form factor boards beyond the card cage for testing, troubleshooting or customer debugging.

Each of these boards meets specific user needs: the BLC-610 provides pin-to-pin extension of the BLC-604 or BLC-614 Card Cage backplane and is fully compatible with the Intel SBC-610; the BLC-8610 retains form, fit and function compatibility with the BLC-610 but adds the dimension of power isolation control.

Power isolation enables the user to remove or insert the board under examination without powering down the entire system and losing instruction functions, status, valuable RAM-stored data, etc. Instead, simply flick the power control switch on the BLC-8610 to remove the power bus from the board being examined.

Test points are visible and easily accessible for examination of all backplane signals and power planes.

Functional Description

When installed in a BLC-604 or BLC-614 Card Cage, the BLC-610 provides uninterrupted feedthrough of each pin on backplane connectors J1 and J2 to a Series/80 board inserted in the BLC-610 connector.

The BLC-8610 contains the same features as the BLC-610 except that two relays are employed to allow the user to switch the power lines on and off, as desired, for testing or removal/insertion of Series/80 boards without fear of damage from transients. Power control does not affect the power supplied to the system except for the small amount of current necessary to drive the relays.

Both boards contain ground lugs tied to system ground via the ground bus from J1 and J2. These lugs are provided as a convenience for grounding test instruments.

Board current may be measured on the BLC-610 by removing jumpers and inserting meter probes used on power runs. On the BLC-8610, de-energized relays are "jumpered" and appropriate metering probes are then inserted on selected power runs.

Specifications

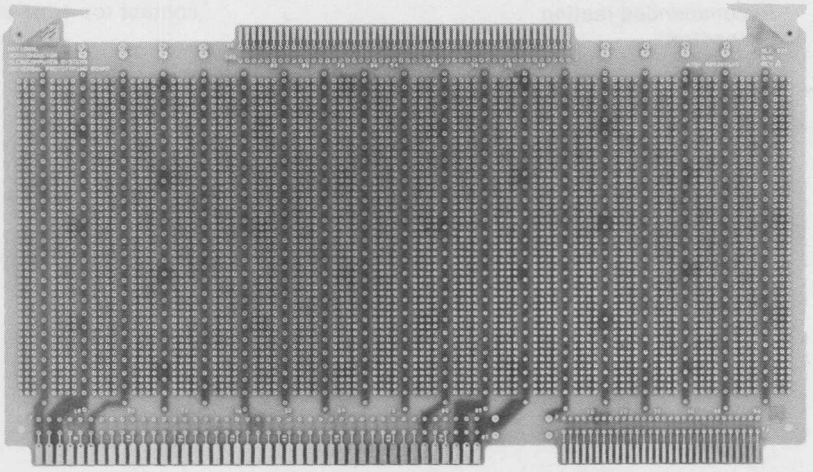
		BLC-610	BLC-8610
Current Rating —	+5V	20A	8A
	−5V	5A	2A
	−10V	5A	2A
	+12V	5A	2A
	−12V	5A	2A
Power —	BLC-610: None required BLC-8610: +12V, 60mA		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	8.00 in.	(20.32 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 g)

Order Information

BLC-610	Extender Board
BLC-8610	Extender Board with Power Control

National Semiconductor

BLC-8905 and BLC-905 Universal Prototyping Boards



BLC-8905

- **Capacity for 108 16-pin DIP's**
- **Choice of Top Edge Connectors**
- **Permits Easier User Construction of Custom Circuitry for BLC/SBC Systems**

Product Overview

The BLC-8905 and BLC-905 provide ready-made, low-cost solutions to the problem of mounting custom circuits in a BLC/SBC computer system. These prototyping boards are designed to accept up to 108 16-pin sockets, integrated circuits, or an equivalent mix of 14, 16, 18, 22, 24, 28, and 40 pin configurations.

Functional Description

The BLC-905 contains one 100 contact top edge connector, and the standard P1 and P2 edge connectors for insertion into a BLC/SBC-604 or -614 card cage backplane.

The BLC-8905 contains two 50 contact connectors and one 26 contact top edge connector.

Specifications

Connectors (BLC-8905)

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers

Parallel I/O — 50 contact double-sided edge connector on 0.10 inch centers

Recommended mating connector:
3M 3415-0001 or equivalent

Serial I/O — 26 contact double-sided edge connector on 0.10 inch centers

Recommended mating connector:
3M 3462-0001 CRIMP or equivalent

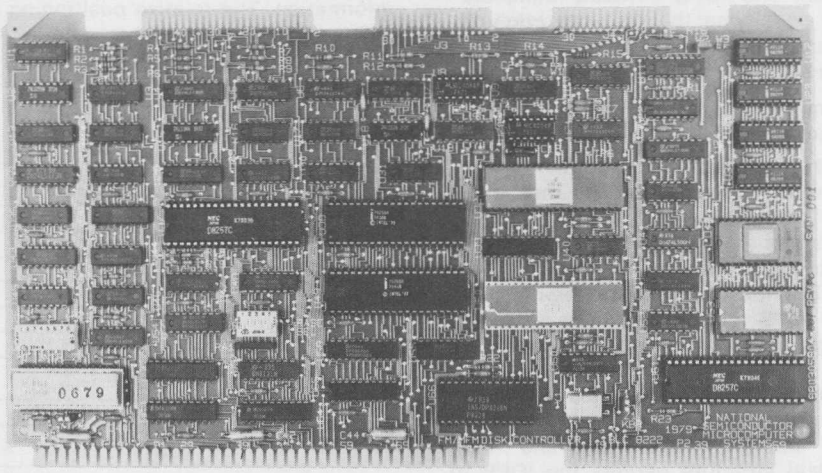
	edge edge connector on 0.156 inch centers		
Top Edge —	100 contact double-sided edge connector on 0.10 inch centers Recommended mating connector: CDC VPB04B50E00A1E		
Environmental	Temperature 0° to 55°C Humidity 0 to 90%, non-condensing		
Physical	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	5 oz.	(141.75 g)

	with one 100 contact top edge connector
BLC-8905	Universal Prototyping Board with two 50 contact and one 26 contact top edge connectors

Section 6
Peripheral Controllers

National Semiconductor

BLC-8222 Double Density Floppy Disc Controller



- **Intelligent Double Density Controller on a Single Series/80 Board**
- **Design Flexibility**
  - Read/Write in IBM System 34 double density (MFM) or IBM 3740 single density (FM) mode
  - FM/MFM selection under program control
  - User definable sector size
  - Switch selectable base addresses allow multiple controller systems
- **Controls Up to Four Dual or Single Sided, Standard or Mini drives**
- **CRC Error Checking with Programmed Re-try**
- **Compatible with Popular Model Shugart Diskette Drives**
- **Bus Transfer Rates Up to 1.3M Bits/Second**

Product Overview

The BLC-8222 Double Density Floppy Disc Controller is a member of National's Series/80 family of intelligent peripheral device controllers. The controller is Multibus™ compatible and provides the Series/80 single board computer user with an easy to use, high performance bulk storage interface. The BLC-8222 uses numerous LSI components, resulting in a powerful single board controller which is economical in terms of space and power consumption, as well as price. Numerous user selectable options are designed in, making the controller highly flexible and easy to use in a wide range of applications requiring large amounts of non-volatile storage.

Functional Description

The BLC-8222 interfaces to the system bus via I/O, DMA, and interrupts. The I/O interface is used to pass information from the system CPU to the controller as well as to allow the CPU to read controller status. The DMA interface is used to transfer control blocks into on-board memory and to transfer data blocks between on-board memory and system memory. The disc controller interrupts are used to inform the system of the completion of operations and changes in disc status.

All diskette operations are initiated by the system processor by standard I/O commands. Once initiated, the disc operations are completed by the

Parameter Block (IOPB) for each operation to be performed. The IOPB contains complete instructions specifying the disc operation. If multiple operations are to be performed, IOPBs can be linked together.

2. Passes the memory address of the IOPB to the controller through two I/O ports.
3. Processes the resultant information from the controller upon completion of the disc operations. The system processor can test for the completion of the disc operation by polling the BUSY status bit through the controller I/O interface or by enabling the controller interrupt through the IOPB and servicing the interrupt generated by the controller.

Operations performed by the disc controller include: read, write, sequential or random format, controller to memory read/write, and test. Controller logical structure permits the IOPB to define command chaining. The system CPU can specify any desired sequence of disc operations and the controller then completes the chained operations autonomously.

Programming

The BLC-8222 appears to the system bus as a set of eight consecutive I/O devices. The I/O addresses range from BASE + 0 to BASE + 7, where BASE is a switch selectable decoding of the upper five I/O address bits. This I/O interface is used by the system processor to send COMMAND bytes to the controller and to read controller STATUS bytes. The relative address decoding and bit assignments for the I/O interface are shown below.

STATUS BYTES

	7	6	5	4	3	2	1	0
BASE + 0	ERROR GROUP				ERROR CODE			
BASE + 1	BUSY	ERROR	RETRY	X	Drive 3 Ready	Drive 2 Ready	Drive 1 Ready	Drive 0 Ready
BASE + 2	X	X	Block tag of last command executed with an error					

INTERFACE COMMANDS

	7	6	5	4	3	2	1	0
BASE + 1	IOPB Memory Address Low							
BASE + 2	IOPB Memory Address High							
BASE + 7	X	X	X	X	X	X	X	X

six or twelve consecutive bytes of control information. The relative positioning of the bytes within the IOPB are as shown below:

IOPB

	7	6	5	4	3	2	1	0
BYTE 1	Disc Number		Interrupt Control		Length	Disk Command		
2	Number of Sectors							
3	Track Number							
4	Sector Number							
5	Buffer Address Low							
6	Buffer Address High							
7	Sector Length							
8	Data Mark		Retry Level		IBM Format	Buffer Start		
9	BTR	X	Block Tag					
10	X	X	Disc Side	X	X	X	DD or SD	CMD Chain
11	Next IOPB Address Low							
12	Next IOPB Address High							

Specifications

Data Word Length —	8 bits parallel
Memory Address Range —	64K bytes
Data Transfer Modes —	DMA, programmed I/O
Data Transfer Rate —	Up to 1.3M bits/second
Data Buffer —	2K bytes
CPU —	INS8080A
Disc Controller —	INS1791
Disc Drive Capability —	4 single or dual sided
Disc Drive Characteristics	
Compatability —	Shugart Models 400, 400L, 800 and 850
Sector Type —	Soft sectored
Recording —	Single or double density
Tracks —	77 for 8 inch standard
Bytes per Sector —	128, 256, or 512 bytes software selectable
Formatted Storage Capacity —	Shugart 400 — 80K bytes 400L — 80K/160K bytes 800 — 256K/512K bytes 850 — 512K/1M bytes
System Bus Interface —	Data, address and command signals are TRI-STATE™ TTL compatible

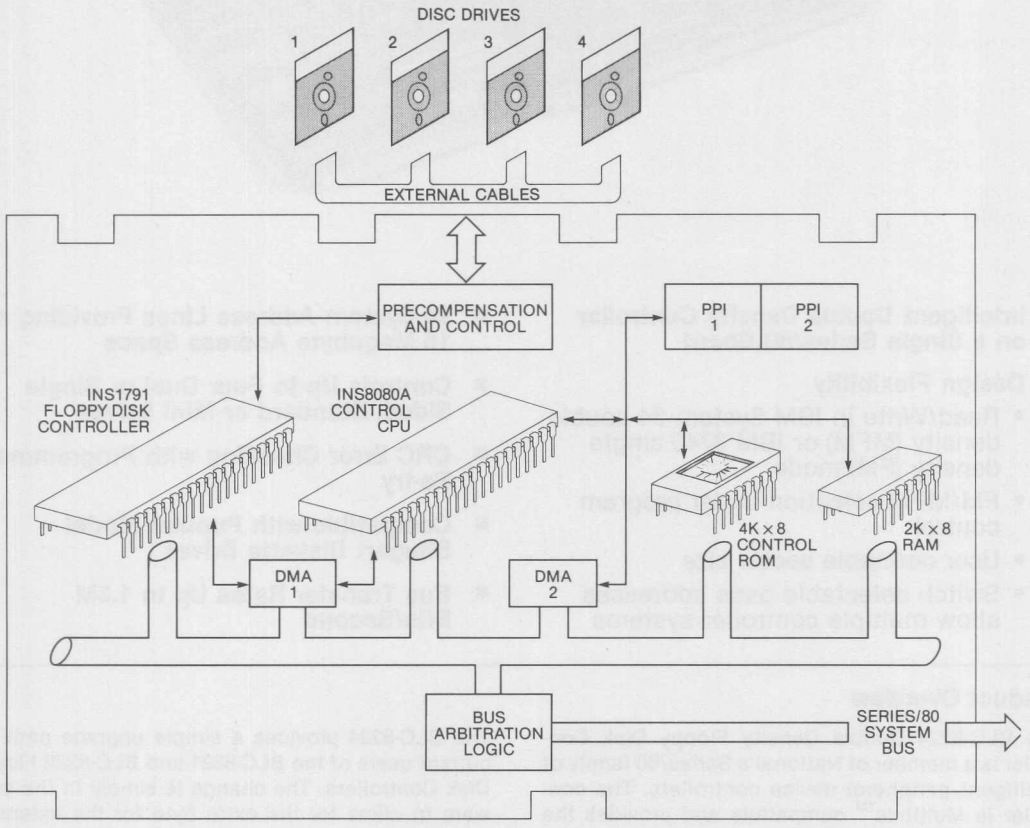
Connectors —	
System Bus	86 contact double sided edge connector on 0.156 inch centers
Auxiliary —	One 60 contact double-sided edge connector on 0.1 inch centers
	Recommended mating connector: 3M "Scotchflex" 3415-0001
Power Requirements —	+5VDC ± 5% 1.75 A +12VDC ± 5% 75 ma −5VDC ± 5% 1 ma
Environmental Characteristics —	Temperature 0 °C to 55 °C Humidity 0–90% non-condensing

Order Information

BLC-8222	Double Density Floppy Disc Controller

Documentation

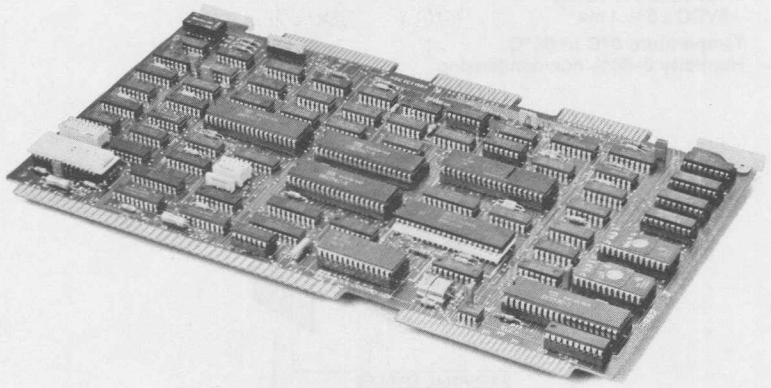
420305804-001	BLC-8222 Floppy Disc Controller Hardware Reference Manual



BLC-8222 DIAGRAM

National Semiconductor

BLC-8224 Double Density Floppy Disk Controller



- **Intelligent Double Density Controller on a Single Series/80 Board**
- **Design Flexibility**
  - Read/Write in IBM System 34 double density (MFM) or IBM 3740 single density (FM) mode
  - FM/MFM selection under program control
  - User definable sector size
  - Switch selectable base addresses allow multiple controller systems
- **24 System Address Lines Providing a 16 Megabyte Address Space**
- **Controls Up to Four Dual or Single Sided, Standard or Mini Drives**
- **CRC Error Checking with Programmed Re-try**
- **Compatible with Popular Model Shugart Diskette Drives**
- **Bus Transfer Rates Up to 1.3M Bits/Second**

Product Overview

The BLC-8224 Double Density Floppy Disk Controller is a member of National's Series/80 family of intelligent peripheral device controllers. The controller is Multibus™ compatible and provides the Series/80 single board computer user with an easy to use, high performance bulk storage interface. The BLC-8224 uses numerous LSI components, resulting in a powerful single board controller which is economical in terms of space and power consumption, as well as price. Numerous user selectable options are designed in, making the controller highly flexible and easy to use in a wide range of applications requiring large amounts of non-volatile storage.

The BLC-8224 provides a simple upgrade path for current users of the BLC-8221 and BLC-8222 Floppy Disk Controllers. The change is simply in the software to allow for the extra byte for the extended addressing range of the BLC-8224. This extension provides an additional eight bits of address (up to 16 megabytes), thus making the BLC-8224 suitable for applications based on 16-bit CPUs.

Functional Description

The BLC-8224 interfaces to the system bus via I/O, DMA, and interrupts. The I/O interface is used to pass information from the system CPU to the

controller as well as to allow the CPU to read controller status. The DMA interface is used to transfer control blocks into on-board memory and to transfer data blocks between on-board memory and system memory. The disk controller interrupts are used to inform the system of the completion of operations and changes in disk status.

All diskette operations are initiated by the system processor by standard I/O commands. Once initiated, the disk operations are completed by the controller with no further interactions. The processor performs the following steps to initiate the complete disk operations:

1. Prepares and stores in system memory an I/O Parameter Block (IOPB) for each operation to be performed. The IOPB contains complete instructions specifying the disk operation. If multiple operations are to be performed, IOPBs can be linked together.
2. Passes the memory address of the IOPB to the controller through two I/O ports.
3. Processes the resultant information from the controller upon completion of the disk operations. The system processor can test for the completion of the disk operation by polling the BUSY status bit through the controller I/O interface or by enabling the controller interrupt through the IOPB and servicing the interrupt generated by the controller.

Operations performed by the disk controller include: read, write, sequential or random format, controller to memory read/write, and test. Controller logical structure permits the IOPB to define command chaining. The system CPU can specify any desired sequence of disk operations and the controller then completes the chained operations autonomously.

Programming

The BLC-8224 appears to the system bus as a set of eight consecutive I/O devices. The I/O addresses range from BASE + 0 to BASE + 7, where BASE is a switch selectable decoding of I/O address bits. This I/O interface is used by the system processor to send COMMAND bytes to the controller and to read controller STATUS bytes. The relative address decoding and bit assignments for the I/O interface are shown below.

Status Bytes

	7	6	5	4	3	2	1	0
BASE + 0	ERROR GROUP				ERROR CODE			
BASE + 1	BUSY	ERROR	RETRY	BYTE 3	Drive 3 Ready	Drive 2 Ready	Drive 1 Ready	Drive 0 Ready
BASE + 2	X	X	Block tag of last command executed with an error					

Interface Commands

	7	6	5	4	3	2	1	0
BASE + 1	IOPB Memory Address Low							
BASE + 2	IOPB Memory Address Mid/High							
BASE + 7	X	X	X	X	X	X	X	X

The start of any diskette operation occurs when the system processor writes to the controller, through I/O addresses BASE + 1 and BASE + 2, the starting address of the IOPB. The IOPB can be located anywhere in main memory and consists of either seven or fourteen consecutive bytes of control information. The relative positioning of the bytes within the IOPB are shown below.

IOPB

	7	6	5	4	3	2	1	0
BYTE 1	Disk Number		Interrupt Control		Length	Disk Command		
2	Number of Sectors							
3	Track Number							
4	Sector Number							
5	Buffer Address Low							
6	Buffer Address Mid							
7	Buffer Address High							
8	Sector Length							
9	Data Mark		Retry Level		IBM Format	Buffer Start		
10	BTR	X	Block Tag					
11	X	X	Disk Side	X	X	X	DD or SD	CMD Chain
12	Next IOPB Address Low							
13	Next IOPB Address Mid							
14	Next IOPB Address High							

Specifications

Data Word Length —	8 bits parallel
Memory Address Range —	16M bytes
Data Transfer Modes —	DMA, programmed I/O
Data Transfer Rate —	Up to 1.3M bits/second

Disk Controller — INS1791

Disk Drive Capability — 4 single or dual sided

Disk Drive Characteristics

Compatability — Shugart Models 400, 400L, 800 and 850

Sector Type — Soft sectored

Recording — Single or double density

Tracks — 77 for 8″ standard

Bytes per Sector — 128, 256, or 512 bytes software selectable

Formatted Storage Capacity — Shugart 400 — 80K bytes
400L — 80K/160K bytes
800 — 256K/512K bytes
850 — 512K/1M bytes

System Bus Interface — Data, address and command signals are TRI-STATE® TTL compatible

Auxiliary — connector on 0.156″ centers
One 60 contact double-sided edge connector on 0.1″ centers
Recommended mating connector:
3M "Scotchflex" 3415-0001

Power Requirements +5 V_{DC} ± 5% 1.75 A
+12 V_{DC} ± 5% 75 mA
−5 V_{DC} ± 5% 1 mA

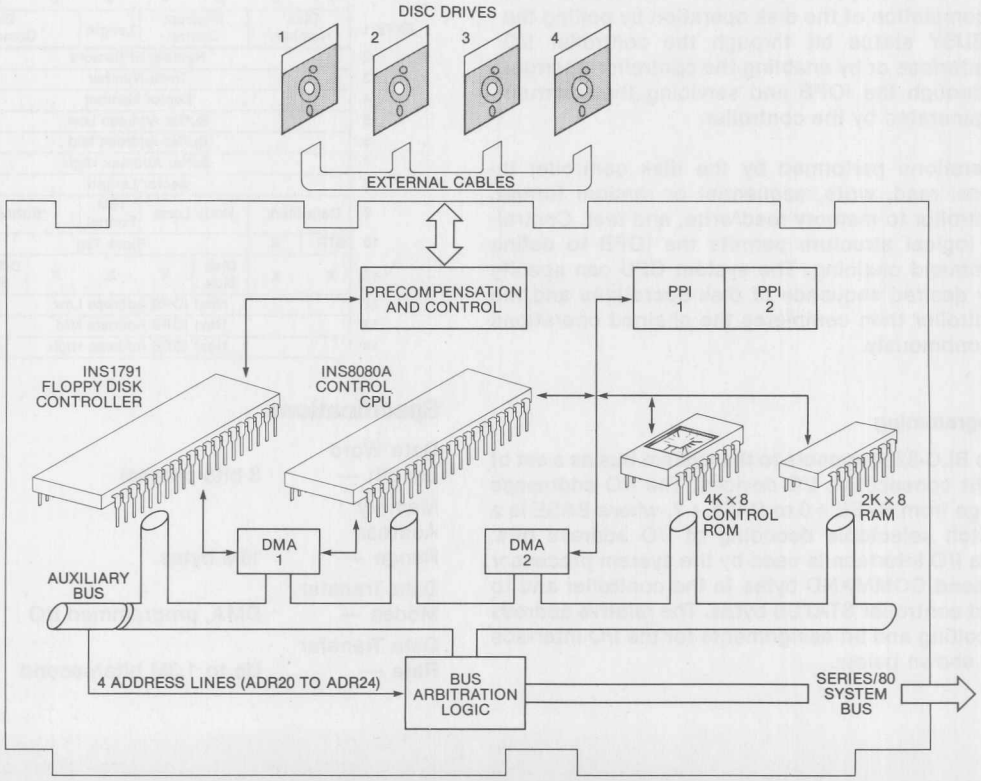
Environmental Temperature 0°C to 55°C
Humidity 0-90% non-condensing

Order Information

BLC-8224 Double Density Floppy Disk Controller

Documentation

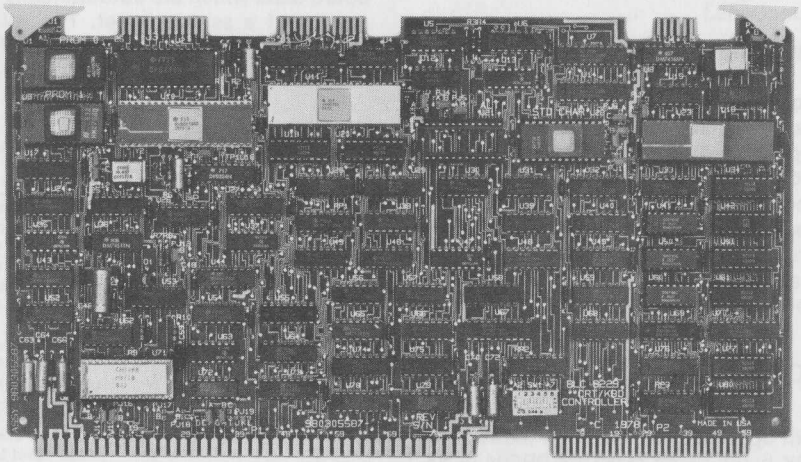
BLC-8224M BLC-8224 Floppy Disk Controller Hardware Reference Manual (Can also be ordered as 420305804-001.)



BLC-8224 Block Diagram

National Semiconductor

BLC-8228 and BLC-8229 Video Monitor/Keyboard Controllers



- **Intelligent Controller on a Single Series/80 Board**
- **Designed for User Flexibility**
  - DMA transfers for rapid screen update
  - Interrupt control
  - On-board 8080A CPU and control ROM
  - 1K byte scratch pad RAM
  - Complete editing function, control logic and scrolling
  - EPROM sockets for user-defined alternate character set
  - Programmable display attributes: blink, blank, inverse video and alternate character set
  - Full software cursor control
  - 3 wire video output
- **On-Board Video Refresh Memory**
- **Full 128 ASCII Character Set**
- **24 Line (BLC-8228) or 25 Line (BLC-8229) by 80 Character Display Array**
- **Selection of Display Matrix**
  - 5 by 7 — BLC-8228
  - 7 by 9 — BLC-8229
- **Compatible with All Series/80 Boards and Card Cages**

Product Overview

The Video Monitor/Keyboard Controller is a member of National's Series/80 family of peripheral device intelligent controllers. It is fully compatible with all National Series/80 boards and plugs directly into any Series/80 card cage backplane or system. The controller is available in two models, BLC-8228 and BLC-8229. The BLC-8228 provides a 5×7 dot matrix character while the BLC-8229 provides a 7×9 dot matrix character.

All that is required to make the BLC-8228 or BLC-8229 an intelligent CRT terminal is the addition of a standard ASCII encoded keyboard and a low cost monitor. The BLC-8228 provides a display array of 24 lines by 80 characters, while the BLC-8229 provides a 25-by-80 array. The character generator consists of a 128 upper and lower case ASCII character set. The controller can also accommodate a user-supplied custom alternate character set which may be software selected on a character-by-character basis.

Full software cursor control (up, down, left, right, home, set, indirect, sense) and screen formatting codes are included to yield a very powerful screen editor. Although on-board firmware provides numerous special editor functions, the user may implement custom editing and formatting functions by writing his own firmware. (See Table I for standard functions.)

Each character is assigned one of four attributes: blink, blank, inverse or alternate character. Scrolling is software selectable for each display line. In this way selected lines can be excluded from scrolling. Non-displayable ASCII control codes (e.g., ACK, EOT, etc.) may be displayed on the monitor and occupy only one display character position. An on-board tone generator is available for connection to an external speaker. The cursor may be represented as block inverse or underscore (blinking or non-blinking).

Functional Description

The BLC-8228 and BLC-8229 contain an on-board 8080A CPU with up to 4 KB of space for instruction ROM/PROM (2K bytes using MM2708 PROM or 4K bytes using MM2716 EPROM), a 1K byte scratch pad RAM, 2K character buffer and 2K×4 bits buffer RAM for character attribute codes, 2K byte refresh RAM, a CRT controller chip, and 2 sockets for a standard and an alternate character generator.

Characters generated by the user's encoded keyboard enter the controller as an 8-bit parallel transfer under interrupt control. The controller transmits the character to the host CPU, which then processes it and transmits it back for display.

Communication between the host CPU and the controller is accomplished in byte parallel via the main system data bus. An 8-bit status register is also available to the host CPU via the main system data bus. Character data can be moved between the controller's RAM buffer and main system memory in DMA mode to provide high speed data transmission.

One of two character generator PROM's (standard or alternate) is enabled according to the state of the controller font bit.

The controller provides 3 host maskable interrupts, CRT Ready, Keyboard Ready and ERROR, to the host CPU. Each of these may be jumpered to any of 9 main bus interrupt lines. The interrupt information is also available to the system by reading the status register contents.

Video output consists of separate horizontal sync, vertical sync and video out signals. STEP-SCAN™ is a jumper selectable option which produces a screen display with more than one line of space between rows and no inter-leaving blank lines between rows and columns. STEP-SCAN is typically used in normal character applications where the extra space produces an exceptionally clear and easy-to-read display.

Controller integrity is assured by execution of on-board tests which are automatically activated upon receipt of a system reset. The validation testing exercises the controller RAM, PROM and I/O display ports.

Table I. Editor Functions and Software Switches (On/Off)

CURSOR	Set Cursor Set Cursor Indirect Set Cursor On Set Cursor Off Sense Cursor Move Cursor Right Move Cursor Left Move Cursor Up Move Cursor Down Move Cursor Home
LINE	Enter Insert Line Insert Line Exit Insert Line Delete Line Erase to End of Line Auto Carriage Return On/Off (80 column)
CHARACTER	Enter Insert Character Insert Character Exit Insert Character Delete Character Destructive Backspace On/Off Upper Case On/Off
TAB	Set Tab Clear Tab Clear All Tabs Back Tab Destructive Tab On/Off Destructive Back Tab On/Off
DMA	Enter DMA Mode Enter DMA With Count Exit DMA Mode Privileged Mode On/Off
SCROLL	Roll Up Roll Down Home & Clear Erase to End of Screen Fix Line Unfix Line Unfix All Lines
ATTRIBUTES	Set Attributes Write Attributes Load Attribute Memory Dump Attribute Memory
SCREEN	Dump Screen Memory Load Screen Memory
MISCELLANEOUS	Write Character Reset Call Subroutine Set LED Set/Reset Software Switches Clear Keyboard FIFO Buffer

7	6	5	4	3	2	1	0
Keybd Ready	CRT Ready	Error Flag					

Error Code

a. Status Register

7	6	5	4	3	2	1	0
Keybd Ready Intrpt Enable	CRT Ready Intrpt Enable	No Error Intrpt Enable	Not Used	Not Used	Not Used	Not Used	Not Used

b. Interrupt Mask Register

7	6	5	4	3	2	1	0
Char/ Control Code							

Data

c. Data Word

Figure 1. Status, Interrupt and Data Format

Specifications

Data Transfer Mode — DMA or Programmed I/O

DMA Transfer Rate — Up to 78K bytes per second

CPU — INS8080A

Video Monitor Controller — DP8350 (5x7)
DP8353 (7x9)

Scratch Pad Buffer — 1Kx8-bit RAM

Attribute Buffer — 2Kx4-bit RAM

Instruction ROM — 2Kx8-bit (standard firmware MM2708)
4Kx8-bit sockets (MM2716 as a user-implemented option)

Character Generator — Standard 128 character upper/lower case ASCII
May also contain user-implemented character set (INS2708 or 2716)

Keyboard Input Port — 8 data lines and 1 strobe from keyboard

Audio Signal Generator — 2500 Hz for 0.15 seconds (BLC-8228)
3300 Hz for 0.15 seconds (BLC-8229)

Special Function Register — 4 bits wide for external LED indicators or custom flags

Display — 24 rows by 80 columns with 5x7 dot matrix (BLC-8228)
25 rows by 80 columns with 7x9 dot matrix (BLC-8229)
Individual character attributes:
- blink (2 Hz)
- blank
- inverse video
- alternate character set

Cursor types (jumper selectable):
- block
- blinking
- non-blinking
- underscore (BLC-8229 only)
- none

Frequency 50 or 60 Hz

Address — Switch select four of 256 available I/O addresses

Bus Interface —

System — Address, data and command signals are TRI-STATE™ TTL compatible

Video Monitor Interface — Horizontal and vertical sync are TTL compatible
Video Out:
- Low — 0.2V
- Med — 1.6V (inverse character background)
- High — 2.2V

Frequency:
- 15.9 KHz (BLC-8228)
- 19.2 KHz (BLC-8229)

Connectors —

System Bus — 86 contact double-sided card cage edge connector on 0.156 inch centers
Recommended mating connector:
- CDC VPB01E43A00A1 or equivalent

Keyboard — 26 contact double-sided edge connector on 0.1 inch centers
Recommended mating connector:
- 3M 3462-0001, TI H3/2113 or equivalent

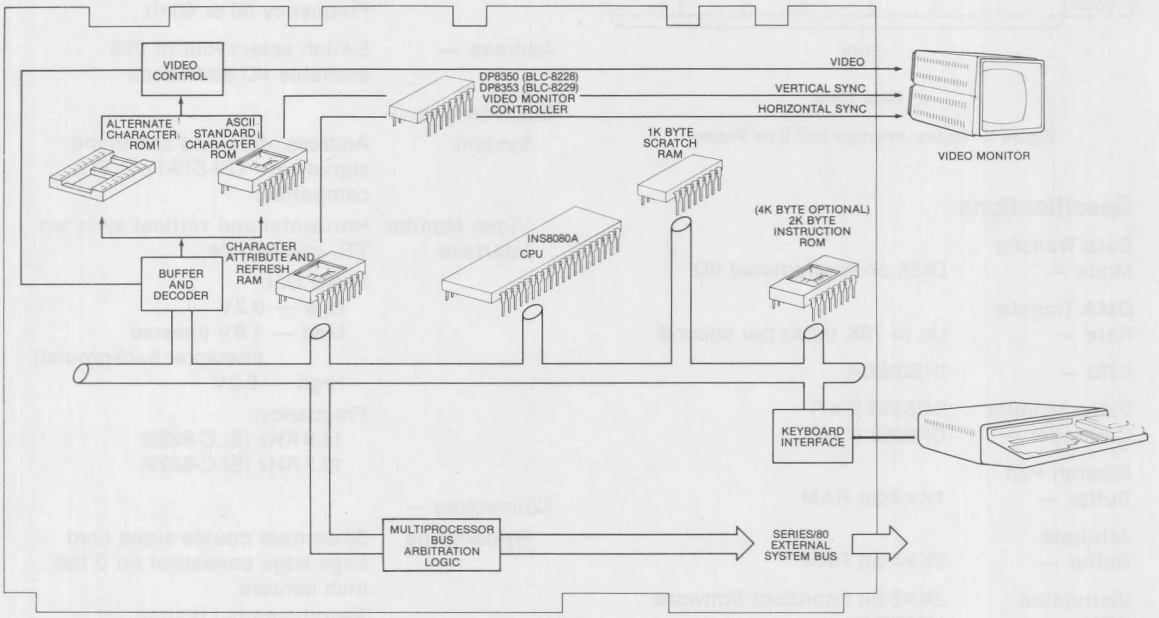
Video Monitor — 12 contact double-sided edge connector on 0.1 inch centers
Recommended mating connector:
- AMP 2-583717-1 or equivalent

	+12V, 0.22A		
	−12V, 0.30A		
Environmental —	Temperature 0° to 55°C		
	Humidity 0 to 90% non-condensing		
Physical —	Height	6.75 in.	(17.15 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	14 oz.	(396.9 g)

BLC-8228	Video Monitor/Keyboard Controller with 5×7 dot matrix character generator
BLC-8229	Video Monitor/Keyboard Controller with 7×9 dot matrix character generator

Documentation

420305587-001	CRT/Keyboard Controller Board Hardware Reference Manual

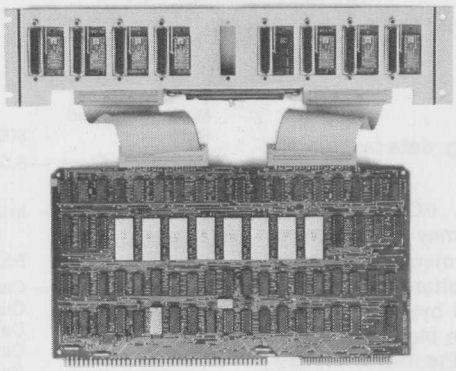


BLC-8228 and BLC-8229 Diagram

Section 7
Communication Controllers

National Semiconductor

BLC-8534 and BLC-8538 Communications Expansion Boards



- **Full Software Parameter Control for Wide Range of Applications**
  - Asynchronous/Synchronous
  - Data format and parity
  - Baud rates to 19.2K
  - Maskable interrupts
  - Modem Control
- **Four or Eight Independently Controlled Channels for Communications System Flexibility**
- **Error Detection for Each Channel**
- **Meets RS232C Interface Standards**

Product Overview

The BLC-8534 and BLC-8538 Communication Expansion Boards are members of National's Series/80 family and are specifically designed to provide flexible multichannel data communications capability for Series/80 BLC/SBC microcomputer systems.

The BLC-8534 and BLC-8538 provide fully independent programmable asynchronous or synchronous serial communication channels conforming to the EIA RS232C standard, thereby allowing connection to a wide variety of data sets and data terminals. Up to eight independent channels are contained on a single board; each is independently programmable to provide the desired channel characteristics.

Two interrupt lines for each channel are provided for communication channel activity sensing.

Functional Description

Channel control is exercised using standard Series/80 instructions and a Universal Synchronous/Asynchronous Receiver Transmitter (USART) circuit for each channel.

Channels are double buffered for full duplex transmission and contain data set control to and from modems. Character framing and transmission mode parameters are controlled by programmable features and BERG™ jumpers.

Transmission Characteristics

- Asynchronous
  - — 5-, 6-, 7- or 8-bit characters
  - — Break character generation
  - — 1, 1½, or 2 stop bits
  - — False start bit detect

— Ring detect

- Synchronous
  - — 5-, 6-, 7- or 8-bit characters
  - — Automatic SYNC character insertion
  - — SYNC search
  - — Baud rate of 50 to 19.2K
  - — External synchronization
  - — Ring detect

Detection is provided for framing, data overrun and data parity errors.

Either standard programmed I/O or memory mapped I/O program control may be employed. Memory mapped I/O permits memory reference instructions to address the channels. Memory mapped I/O uses a block of 64 bytes of memory; the base address of any 64 byte block is selected using switches on the board. Electronic Industry Association drivers and receivers are used to insure electrical compatibility of channel interfaces.

Interrupts

Two interrupt lines for each channel are available to notify the system CPU when input data is available for transfer (input buffer full), and when data has been transmitted to the serial line (channel output buffer empty). They are individually maskable under program control, allowing a high degree of channel control flexibility. The interrupts may be OR tied or individually sensed, depending on the CPU used or the method of application.

Connectors

An optional connector kit is available to alleviate the need for special user cabling. The kit consists of a connector board which receives up to four RS232C connectors. The board is designed so that each of the four connectors may be user switched from either a terminal or a modem interface. A cable is provided to connect the BLC-8534/8538 to the connector board. The conector boards may be mounted on the back of a rack mounted computer using a special RMC back panel or on a 19 inch rack using the optional RETMA panel.

Channels —	4 or 8
Mode —	Full duplex
Control —	Independent channel
Standard Baud Rates —	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200
Maximum Baud Rate —	800 KHz
Baud Rate Clock —	5.068 MHz
Baud Rate Synchronization —	Internal or external
Interface Standard —	RS232C
Interface Signals —	Carrier Detect Clear to Send Data Set Ready Data Terminal Ready Request to Send Receive Clock Transmit Clock Transmit Data Receive Data Ring Indicator
System Bus Interface —	Data, address and command signals are TRI-STATE™ compatible
Connectors	
System Bus —	86 contact double-sided card cage edge connector on 0.156 inch centers
Serial Channel —	Two 50 contact double-sided edge connectors on 0.1 inch centers Recommended mating connector: 3M 3415-0001 AMP 2-86792-3

Power —	Voltage	8534	8538
	+5V	2.0A	2.9A
	+12V	0.13A	0.25A
	−12V	0.12A	0.23A

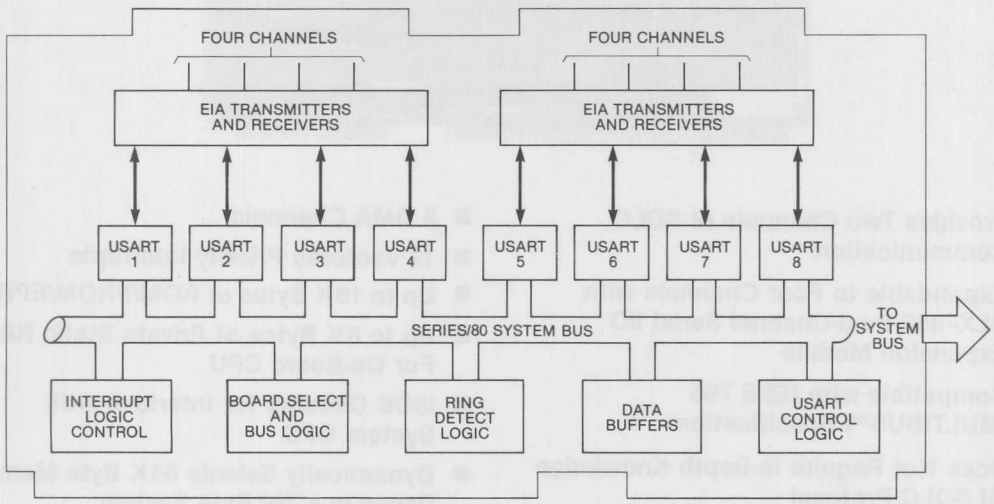
Environmental —	Temperature 0° to 55°C		
	Humidity 0 to 90% non-condensing		
Physical —	Height	7.05 in.	(17.91 cm)
	Width	12.00 in.	(30.48 cm)
	Depth	0.50 in.	(1.27 cm)
	Weight	12 oz.	(340.2 gm)

Order Information

BLC-8538	Eight Channel Communications Expansion Board
BLC-8958	RMC Communications Line Connector Kit (6 in. cable)
BLC-8958-1	RETMA Communications Line Connector Kit (15 ft. cable)
RMC-A001	RMC Communications Back Panel
AEE-001	RETMA Communications Termination Panel

Documentation

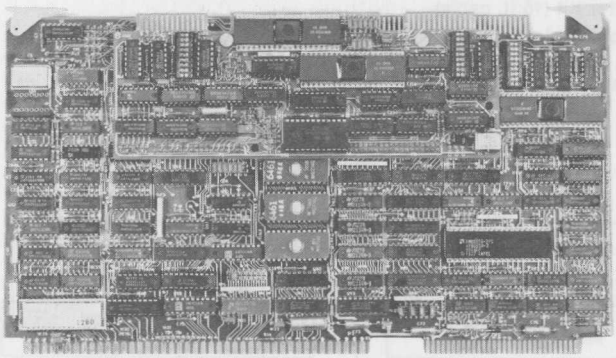
420305528-001	BLC-8534/8538 4 and 8 Channel Communications Expansion Boards Hardware Reference Manual



BLC-8538 DIAGRAM

National Semiconductor

BLC-8545
Intelligent Communications Controller Board



- **Provides Two Channels of SDLC Communication**
- **Expandable to Four Channels with BLX-355 Dual-Channel Serial I/O Expansion Module**
- **Compatible with IEEE 796 (MULTIBUS™) Specification**
- **Does Not Require In-Depth Knowledge Of SDLC Protocol**
- **Full Duplex, Transfer Rate Selectable From 75 to 19200 Baud**
- **8 DMA Channels**
- **12 Vectored Priority Interrupts**
- **Up to 16K Bytes of ROM/PROM/EPROM**
- **Up to 6K Bytes of Private Static RAM For On-Board CPU**
- **IOCB Circuitry for Interface with System CPU**
- **Dynamically Selects 64K Byte Memory Pages in a 1M Byte System**
- **Compatible with Industry Standard BLC/SBC Hardware and Software**

Product Overview

The BLC-8545 Intelligent Communications Controller Board provides two channels of IBM-SDLC protocol communication on one board, and allows for expansion to four channels with the addition of the BLX-355 Dual-Channel Serial I/O Expansion Module. The BLC-8545 interfaces to the MULTIBUS as a bus multimaster and performs communication between the on-board CPU and a system central processor via Input/Output Control Blocks (IOCBs). Because of the BLC-8545's own intelligence and the IOCB facility, the user need not have in-depth knowledge of the SDLC protocol. He need only configure the IOCB and then let the BLC-8545 control the communication.

The data rate for the two channels may be selected from 75 to 19200 baud in full duplex mode. Data transfer between the I/O ports and system memory or the on-board RAM can be done by polling, interrupting, or direct memory access (DMA). All control functions are carried out by on-board firmware.

The BLC-8545 is equipped with a number of options that are selectable by on-board jumper connections:

- Clock frequencies
- Multimaster configuration
- RAM/PROM size and mix
- NRZI encode/decode
- Interrupt selection
- IOCB base address
- Ring indicator and carrier detect
- TTY adaptor power and ground

MULTIBUS is a trademark of Intel Corp.

Functional Description

Central Processor

The central processor on the BLC-8545 is the 8085A-2. The 8085A-2 is a member of a generation of high-speed 8-bit microprocessors. Running at a speed of 4.9152MHz, it is capable of a minimum instruction time of 0.812μs (4 clock cycles).

Memory

Three sockets are provided on the BLC-8545 which are capable of supporting either 1K×8 (2716) or 2K×8 (2732) PROMs. An additional socket may be loaded with either PROM (2716 or 2732) or RAM (6116 or equivalent). There is an additional 4K bytes of static RAM on the board serving as the minimum required for any configuration of channels/protocols. Jumpers are provided for board set-up for any available mix of RAM and PROM. Maximum allowable amounts are 16K bytes of PROM with 4K bytes of RAM, and 12K bytes of PROM with 6K bytes of RAM. Future protocols for the BLC-8545 may be added by simply replacing the PROMs.

Input/Output

Serial data transfers are carried out through two SIO ports compatible with either RS232C or CCITT/V.24 standards. Data transfer may be effected by an information exchange between the on-board CPU and the serial interface by an interrupt-drive process, or by direct memory access.

The BLC-8545 is capable of directly addressing 256 input ports and 256 output ports, optionally selectable to 512 input and output ports. Two ports are accessed by the MULTIBUS™ for IOCB operation with their I/O address assignments being jumper-selectable.

The MULTIBUS interface, which provides communication between the BLC-8545 and the system controller, includes capabilities for bidirectional address buffers, command lines, acknowledge circuitry, multimaster bus control logic, IOCB circuitry, and timing.

DMA

Eight channels of direct memory access are provided by two DMA controller devices. The DMA controllers permit the full-duplex DMA transfer of data between the two SIO ports, or the two BLX connectors, and the system memory, or the on-board CPU.

Interrupts

Eight data transfer interrupts (in addition to four interrupt vectors from the CPU) are provided by a programmable interrupt controller (PIC). The PIC generates a CALL instruction that enables the on-board CPU to point to any interrupt service routine in memory. The PIC arbitrates among interrupt requests and services them on a programmed scheme of a first-come, first-served basis.

The BLC-8545 can issue an interrupt to the MULTIBUS to signal the completion of a command. This interrupt is jumper-selectable to any of the eight available on the bus.

Board Operation

Upon power-up, firmware on the BLC-8545 resets the on-board circuitry, establishes the board's configuration as determined by the options selected, and reports its status back to the system controller.

Control/response information is passed between the system controller and the BLC-8545 by means of IOCBs. The general IOCB structure is illustrated below.

Byte	Bit 7	6	5	4	3	2	1	0
00	IOCB Type (000)				Operation ID			
01	Opcode							
02	IOCB Status							
03	Buffer Address (Low)							
04	Buffer Address (Middle)							
05	Reserved				Buff. Addr. (High)			
06	Transfer Length (Low)							
07	Transfer Length (High)							
08	Depends on Opcode							
09								
10								
11								
12								
13								
14	Timer (Low)							
15	Timer (High)							

The IOCB type and operation ID fields (byte 0) are for the user to "tag" the IOCB for later identification, if desired. The opcode field defines whether the IOCB refers to a command or a request for status. The IOCB status (byte 2) reports the status of the IOCB (as opposed to board status). The system address bytes (3–5) indicate the system memory location where commands or data are located or the address where commands will be stored or data will be transferred. IOCB bytes 6 and 7 indicate the data transfer length for the frame of SDLC data. The information contained in bytes 9–13 relates specifically to the opcode. A timer may be set in bytes 14 and 15 to indicate how long the controller should wait for an event to take place or how long an operation should continue.

Initialize controller	INIT	40
Transmit	TRAN	81
Receive data	RECV	82
Disconnect station	DISC	83
Request disconnection	RQDC	84
Exchange identification	EXID	85
Test station	TEST	86

The information transferred in SDLC format serves two functions: it establishes the "link" — the communication path between the transmitter and receiver — as well as transferring the desired data itself. A single SDLC communication element, called a frame, can be graphically represented as shown below.

Flag (8)	Address (8)	Control (8)	Information (Varies)	Frame-Check Sequence (16)	Flag (8)

The elements of a frame are a beginning 8-bit flag; an 8-bit address field; an 8-bit control field; a variable-length information field; a 16-bit frame check sequence for error detection; and an ending flag, which has the same bit-pattern as the beginning flag.

BLX Connectors

All signals required for operation of a BLX-355 Dual-Channel Serial I/O Expansion Module are present at the BLX connectors at all times. Adding a BLX-355 for expansion to 4 SIO channels is simply a matter of plugging the board in. No further adjustments or modifications are necessary.

If resources other than synchronous serial I/O are desired, then any BLX Expansion Module from the Series/80 line may be used. These resources include, fixed and/or floating point math, parallel I/O, speech synthesis, analog I/O, and others.

System clock	4.9152 MHz
Minimum instruction time	0.812 μs (4 clock cycles)
Address capacity	1M byte, divided into 16 64K byte pages

Memory

ROM/PROM/ EPROM	3 sockets supporting 2716 or 2732
RAM	4K bytes static RAM for use by on-board CPU
RAM/PROM	1 socket supporting 2716, 2732, or 6116

Input/Output

Interrupts	12 vectored priority interrupts, including CPU NMI
Data and addressing	IOCB circuitry for interfacing between on-board CPU and system CPU
SIO	SDLC protocol output through RS232C or CCITT/V.24 interface
DMA	8 channels
Baud rate	Selectable 75 to 19200, full duplex, on four channels
System bus	Compatible with MULTIBUS™ specifications. All interface signals are TTL compatible.

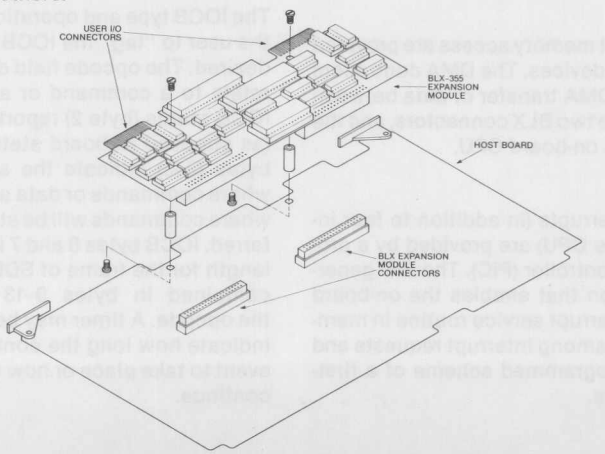


Figure 1. BLC-8545 with BLX-355 Dual SIO Expansion Module Installed

Power

Configuration	Current Requirements (Max.) +5V±5%	+12V±5%	−12V±5%
No PROM	4.4A	70mA	46mA
8K EPROM (2716)	4.8	70	46
16K EPROM (2732)	5.0	70	46
Aux. power	475mA	0	0
BLX-355	730	70	46

Environmental

Temperature: 0°C to 55°C
Humidity: 0% to 90% noncondensing

Physical

Height: 6.75 in. (17.15 cm.)
Width: 12.00 in. (30.48 cm.)
Depth: 0.50 in. (1.27 cm.)
Weight: 17.5 oz. (496 gm.)

Connectors

System bus

86-contact, double-sided, card-edge connector on 0.156 inch centers. Recommended mating connectors:

Soldered

DCD	VBP01E43D00A1E
μPlastics	MP-0156-43-BW-4
ARCO	AE443WP1 (Less ears)
Viking	2VH43/1AV5

Wirewrap

CDC	VFB01E4D00A1
Viking	2VH43/1ANE5

Auxiliary bus

60-contact, double-sided, card-edged connector on 0.100-inch centers. Recommended mating connectors:

Soldered

Viking	3VH30/ljn75
TI	H321130

Wirewrap

CDC	VPB01830DOA1

Serial I/O

26-contact, double-sided, card-edge connector on 0.100-inch centers. Recommended mating connectors:

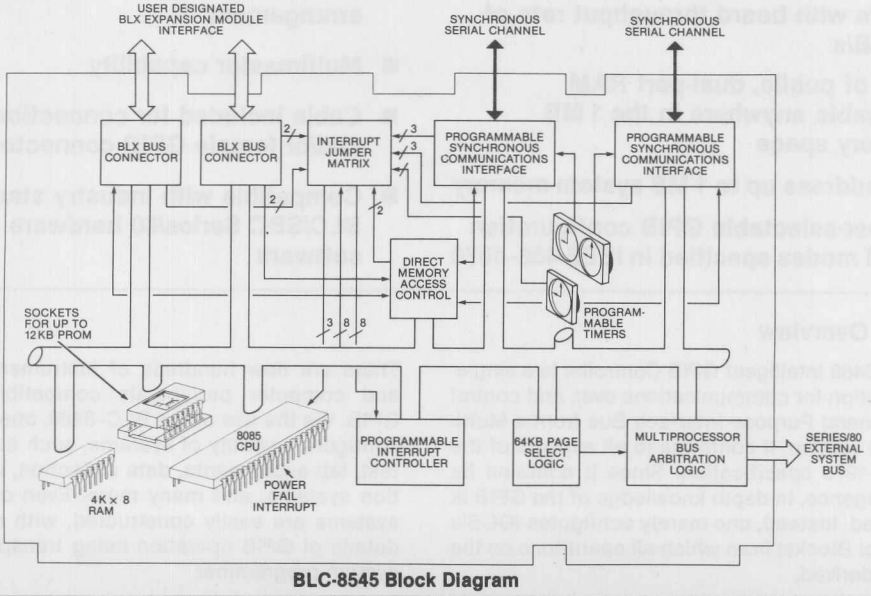
3M	3462-000

Order Information

BLC-8545	BLC-8545 Intelligent Communications Controller Board, includes on-board firmware for support of SDLC protocol

Documentation

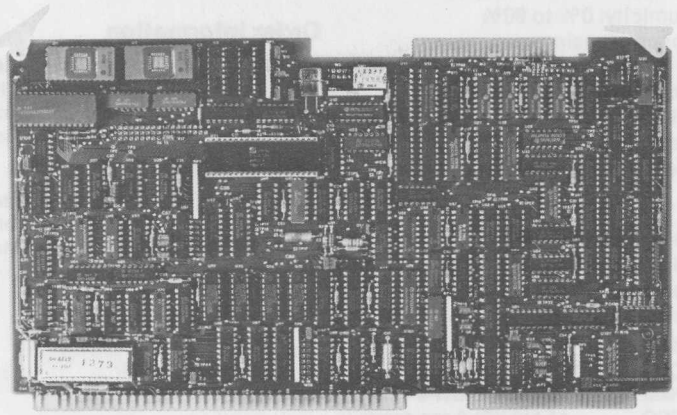
BLC-8545M	BLC-8545 Intelligent Communications Controller Board Hardware Reference Manual (420306343-001)



BLC-8545 Block Diagram

National Semiconductor

BLC-8488
Intelligent GPIB Controller Board



- **Provides communications between GPIB-compatible instruments/devices and the Multibus™**
- **Does not require in-depth knowledge of GPIB**
- **Conforms to IEEE standard 488-1978 interface**
- **Maximum GPIB data transfer rate of 1 MB/s with board throughput rate of 125 KB/s**
- **2 KB of public, dual-port RAM mappable anywhere in the 1 MB memory space**
- **Can address up to 1 MB system memory**
- **Jumper-selectable GPIB configuration for all modes specified in IEEE 488-1978**
- **Primary and secondary address handling capability**
- **Up to 8 KB of ROM/PROM control firmware storage (only 4 KB required by supported firmware)**
- **1 KB of private RAM**
- **Flexible interrupt handling/generation arrangement**
- **Multimaster capability**
- **Cable included for connection to male and/or female GPIB connectors**
- **Compatible with industry standard BLC/SBC Series/80 hardware and software**

Product Overview

The BLC-8488 Intelligent GPIB Controller is a single-board solution for communications over, and control of, the General Purpose Interface Bus from a Multibus-based system. It conforms to all aspects of the IEEE 488-1978 specification. Since it contains its own intelligence, in-depth knowledge of the GPIB is not required. Instead, one merely configures IOCB's (I/O Control Blocks) from which all operations on the GPIB are derived.

There are now hundreds of instruments, devices, and computer peripherals compatible with the GPIB. Via the use of the BLC-8488, one can quickly configure a variety of systems, such as production test, lab experiments, data collection, instrumentation systems, and many more. Even one-shot test systems are easily constructed, with many of the details of GPIB operation being transparent to the system programmer.

Multibus is a trademark of Intel Corp.

The BLC-8488 provides jumper selection for the following GPIB configurations:

- Talker only
- Listener only
- Talker/listener
- Controller
- System controller
- Extended talker
- Extended listener
- Extended talker/ extended listener
- Talker
- Listener

The BLC-8488 supports the following IEEE 488-1978 GPIB protocols:

- Hardware implementation of Source (SH1) and ACCEPTOR (AH1) handshake
- Firmware implementation of TALKER (T5,TE5), LISTENER (L3,LE3), TALKER/LISTENER (T5,TE5, L3,LE3), CONTROLLER (C4,C5), SYSTEM CONTROLLER (C1,C2,C3,C4,C5), SERVICE REQUEST (SR1), REMOTE/LOCAL (RL1), PARALLEL POLL (PP2), CLEAR DEVICE (DC1), and DEVICE TRIGGER (DT1).

A maximum data throughput rate of 125 KB/s is accomplished by the utilization of an on-board Z-80A microprocessor, 2K bytes of public dual port RAM mappable anywhere within the 1 MB memory space, and discrete implementation of the GPIB interface.

The system contains a flexible interrupt handling arrangement, including:

- Reception of Service Request signal from IEEE 488 Bus to be locally processed (Controller Function).
- Generation of Service Request signal to IEEE 488 Bus (Serial Poll (SR) Function).
- Reception of one of the eight interrupt levels on Multibus (Jumper Selectable).
- Generation of one interrupt to one of the eight Multibus interrupt levels (Jumper Selectable).

The BLC-8488 has multimaster capability. As such, it can gain access to the shared resources on the Multibus depending on its own priority on the Multibus.

Functional Description

Central Processor

The BLC-8488 uses the Z-80A as its CPU. The Z-80A is not only compatible with existing 8080 code, but also offers several other advantages. The instruction set for the Z-80A has been expanded to 158 (vs. 78 for the 8080), providing more power in the same code space. Twelve registers have been added to the 8080 complement for a total of 22.

Memory

ROM/PROM

Two sockets are provided on the BLC-8488 supporting 2708, 2716, and 2732 devices.

Dual-Port RAM

Two kilobytes of static RAM are available to both the on-board Z-80A and the Multibus. The address for the Multibus interface can be put on any 2 KB boundary within the 1 MB address space. Base address for the Z-80A is at 2000_H.

Private RAM

One additional kilobyte of static RAM is provided and dedicated to the on-board Z-80A. It is located at 2800_H.

Input/Output

The Z-80A has the ability to address 256 input ports and 256 output ports. On the BLC-8488, several I/O addresses have been assigned to on-board resources: the GPIB data interface, and an 8259 Programmable Interrupt Controller (PIC). All others are available for use off-board in any manner the user defines.

The BLC-8488 requires two I/O addresses on the Multibus for passing location information about the IOCB. They can be defined on any even-byte boundary from 0_H to FE_H.

Interrupts

The PIC can receive, mask, and resolve priority on up to eight interrupt inputs. Along with several interrupt lines for the GPIB interface, a jumper matrix allows selecting any one of the eight Multibus interrupt lines for input to the PIC. An interrupt can also be generated by the BLC-8488 and output on any one of the Multibus interrupt lines.

Multimaster

The BLC-8488 is a full multimaster. As such, it can assume control of the Multibus in the same fashion as any Series/80 CPU board. Off-board resources (digital and I/O expansion boards, memory expansion boards, peripheral controller boards, other CPU boards) can therefore be used/controlled by the BLC-8488. By virtue of its dual-port RAM, it can also be treated as a Multibus slave. This flexibility allows the BLC-8488 to be used in any system architecture.

Board Operation

Upon application of power to the BLC-8488, the firmware supplied with the board reports the board busy, resets the on-board circuitry, reads the GPIB configuration switches and sets up the necessary modes, programs the PIC, reports the GPIB configuration, and readies itself to handle activity on either the Multibus or the GPIB.

The host CPU board (in a multiprocessor system) builds an IOCB (see Figure 1). The IOCB's address (can be in the dual-port RAM or other shared memory) is passed to the BLC-8488 by an I/O write. The BLC-8488 then DMA's the IOCB into its private RAM and executes the operation. Received data is placed

use of the dual-port RAM for shared memory (IOCB, GPIB status, and transmit/receive data). This allows all operations to occur without the BLC-8488 having to contend for bus control.

	Content							
	7	6	5	4	3	2	1	0
Byte 0	IOCB Type			Operation ID				
1	Opcode							
2	IOCB Status							
3	System Memory Address (Low Byte)							
4	System Memory Address (Middle Byte)							
5	System Memory Address (High Byte)							
6	Reserved							
7	Reserved							
8	Serial Poll Status							

BLC-8488 — IOCB Format

The IOCB type and the Operation ID fields (Byte 0) are for the user to "tag" his IOCB's for later identification, if desired. The Opcode field (Byte 1) defines whether this IOCB refers to a command or a request for status. IOCB Status (Byte 2) reports the status of the IOCB, versus the status of the GPIB or of the BLC-8488. System Memory Address (Bytes 3-5) is a pointer to the location in shared memory where commands or GPIB data are to be found, or where status or GPIB data are to be stored. Serial Poll Status (Byte 8) is used to report the result of a request for status of the GPIB. Bytes 6 and 7 are reserved.

There are five general groups of commands that the supplied firmware can execute. Examples of these are the data transfer group and the GPIB controller commands group. Within each general group are numerous commands actually used to carry out operations on the GPIB and control the BLC-8488. Some commands within the GPIB controller group, for instance, are: all devices clear, send control to a specified controller, and assign talker/listener address. Naturally, a thorough discussion of the commands is provided in the BLC-8488 Hardware Reference Manual.

There are two types of status reported by the BLC-8488: GPIB status and BLC-8488 status. GPIB status is reported in shared memory. BLC-8488 status is reported in the I/O space dedicated to this board. Definition of all status bits becomes too involved for the scope of this data sheet. The BLC-8488 Hardware Reference Manual provides a rigorous discussion of both status types, as well as all other aspects of the board.

male or female connection to the GPIB. Additional hardware is supplied to bulkhead mount the GPIB end of the BLC-8988 to the rear panel of a Series/80 RMC (rack mountable chassis) unit, if desired.

Specifications

Microprocessor

CPU — Z-80A

Data Word — 8 bits

Instruction Word — 8, 16, 24 bits

System Clock — 3.08 MHz ± 0.1%

Minimum Instruction Time — 1.29 μs (4 clock cycles)

Address Capacity — 64K bytes

Memory

ROM/PROM — 2 sockets
2708 — 0_H to $7FF_H$
2716 — 0_H to FFF_H
2732 — 0_H to $1FFF_H$

Private RAM — 1 KB, 2800_H-$2BFF_H$

Dual-Port RAM — 2 KB
Internal access, 2000_H-$27FB_H$,
Multibus access, any 2 KB boundary within 1 MB

Input/Output

Interrupts — 9 levels, hardware vectored (1 output available)

Multibus — 2 I/O address on any even boundary within 0_H-FE_H (0_H-1FE in 16-bit system)

On-Board I/O — GPIB I/O — $D0_H$-DB_H
8259 — DC_H-DF_H

Memory Mapped I/O — $2BFC_H$-$2BFF_H$

GPIB

Data Transfer Rate — 1 MB/s

Data Throughput Rate — 125 KB/s

IEEE Compatibility — Meets IEEE 488-1978

System Bus Multiple bus master capability for up to 6 masters, expandable to 16 masters with additional priority network. All address data and control signals are TRI-STATE® TTL compatible.

Connectors

System Bus — 86-contact, double-sided, card-edge connectors on 0.156″ centers

Recommended mating connectors:

Soldered

DCD	VPB01E43D00A1E
μ Plastics	MP-0156-43-BW-4
ARCO	AE443WP1 (Less ears)
Viking	2VH43/1AV5

Wirewrap

CDC	VFB01E4D00A1
Viking	2VH43/1ANE5

Auxiliary Bus — 60-contact, double-sided, card-edge connectors on 0.1″ centers

Recommended mating connectors:

Soldered

Viking	3VH30/1jn75
TI	H321130

Wirewrap

CDC	VPB01B30D00A1
TI	H311130
AMP	PE5-14559

GPIB — 50-contact, double-sided, card-edge connector on 0.1″ centers

Recommended mating connector:

NSC	BLC-8988 (BLC-8488 to IEEE 488-1978 interconnect)

Power

Current Requirements (Max.)

Configuration	+5V ± 5%	−5V ± 5%	+12V ± 5%
With 2708's	2.6 A	120 mA	160 mA
With 2758's, 2716's, 2732's	2.6 A	—	—

Environmental Temperature — 0°C to 55°C
Humidity — 0% to 90%, non-condensing

Physical

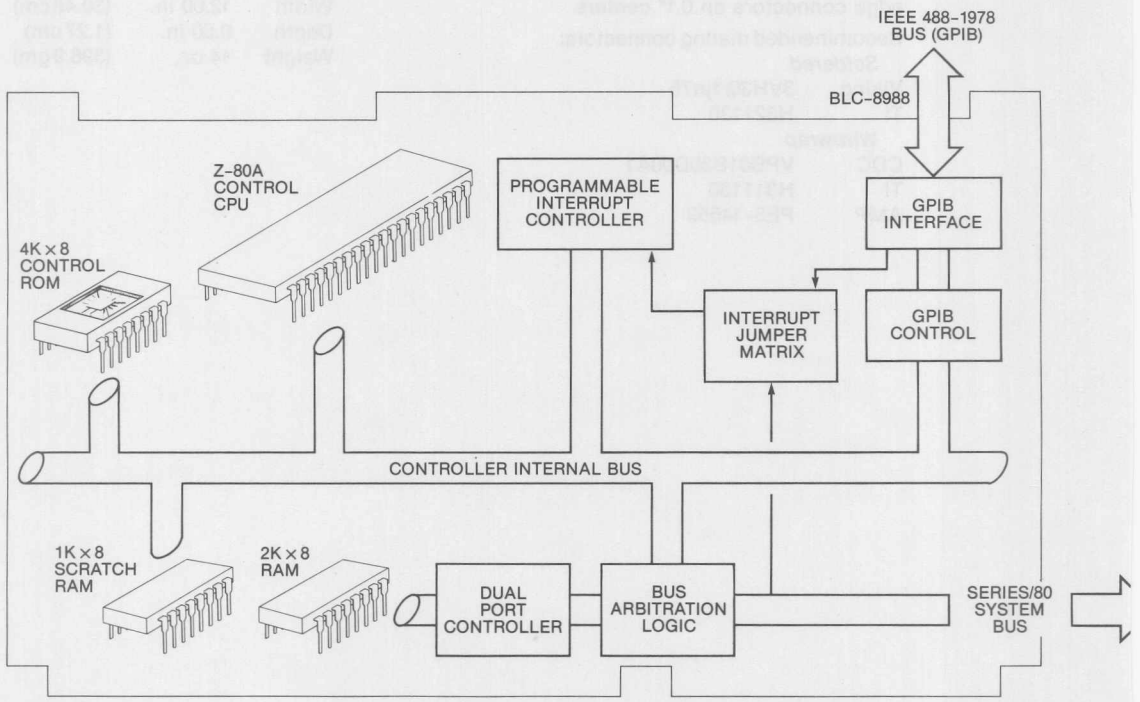
Height	6.75 in.	(17.15 cm)
Width	12.00 in.	(30.48 cm)
Depth	0.50 in.	(1.27 cm)
Weight	14 oz.	(396.9 gm)

Order Information

BLC-8488	Includes BLC-8488 Intelligent GPIB Controller Board, BLC-8988 interface cable, IOCB-compatible firmware for multiprocessor system, and one year warranty on service and parts
BLC-8988	BLC-8488-to-GPIB interface cable (one is provided with order of BLC-8488)

Documentation

420306095-001	BLC-8488 Intelligent GPIB Controller Board User's Manual

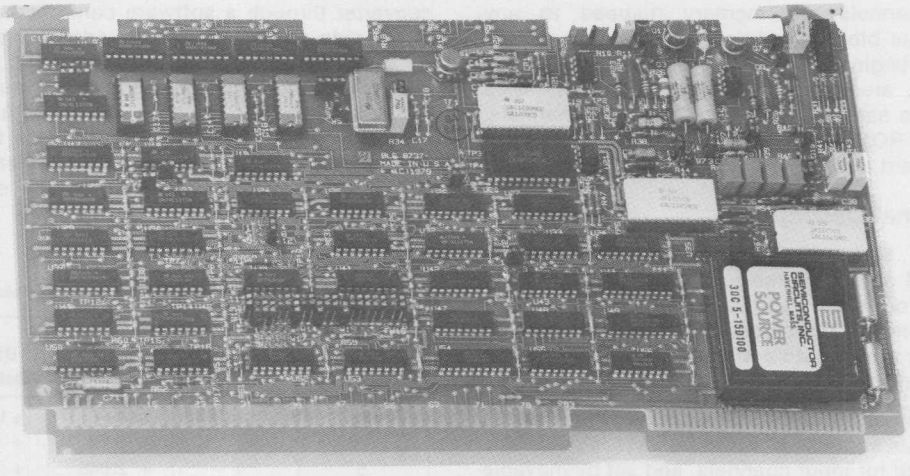


BLC-8488 Block Diagram

Section 8
Analog I/O Boards

National Semiconductor

BLC-8737
Analog Input/Output Board With Memory



- **Mailbox Bus Interface**
  - Latest data from all channels stored on-board
  - Gains need be set only once
  - Simple memory reference instructions to read data or set gains
- **Application Flexibility**
  - 16 single-ended/8 differential channels
  - Expandable to 32 single-ended/16 differential channels
  - 2 output channels
  - Provisions for 4-20ma inputs and outputs
  - Programmable gain amplifier
  - Sequential scan or CPU-driven selected channel conversions
  - Input protection up to 125VAC
- **12-Bit Resolution With ±0.05% Overall Input and Output Accuracy**
- **4-20ma True Current Sourcing Output Channels Permit Grounded Loads**
- **Single 5V Power Required**

Product Overview

The BLC-8737 analog I/O Board with memory extends the Series/80 family of microcomputer products into a wide variety of instrumentation and process-control applications, yet minimizes the data interfacing software because of the on-card memory. Multiple analog input and output capability is provided.

The BLC-8737 makes each input channel appear to be a RAM address. Data is read by a single memory-read instruction at normal memory speeds. Writing into that address once will set the gain on that channel until reset to a different gain by a subsequent write (gain) instruction.

Analog inputs are automatically sampled in sequential repetitive mode. However, a gain-set write instruction will re-start the scan at that channel. This mode, together with an interrupt output, allows random or equivalent single-channel operation when desired. The throughput rate is 8500 channels/second, and is adequate for most process/instrumentation systems with data bandwidth to 100/200/400 Hz on each of 32/16/8 channels.

The input circuitry contains 16 single-ended or 8 differential-channel multiplexers, input protection on each channel, a fast-settling differential (instrumentation) amplifier with software programmable gain, sample-and-hold amplifier, a 12-bit analog-to-digital converter, voltage reference, gain-program memory, and 32-channel data memory. The input may be expanded to 32 single-ended or 16 differential channels.

The output circuitry contains two 12-bit digital-to-analog converters with latched input registers, a precision voltage reference with offsetting circuitry, and two 4-20ma voltage-to-current converters with true current sourcing to permit grounded loads.

Input channels are memory mapped to any contiguous block of addresses which are jumper selected beginning with an even address. Output channels are memory mapped anywhere else within the same 2K block as the input channels. RAM and ROM inhibit signals are provided, should the I/O card address overlap installed memory.

Functional Description

Standard Series/80 instructions control analog input and output. Memory mapped I/O and single memory-reference read and write instructions greatly simplify the programming task and reduce computer timing load compared with other analog I/O systems.

With memory mapped I/O, a segment of 32 contiguous addresses (16 double-byte locations) is predefined for input channels, and set by movable jumpers on the board. These addresses may be on any given 32-byte boundary within the 64 K bytes of available address space. These addresses overlay system memory address functions with memory inhibit logic to prevent address contention for memory-mapped I/O addresses. Output channels share the same six most significant address bits with input addresses, however, they may be jumper selected to any other block of 16 locations within the same 2K space occupied by the input channels.

Analog Input

The card normally operates in a sequential scan mode with a 118 microsecond period devoted to each channel. This allows settling time for the multiplexer, instrumentation amplifier, and S/H amplifier ADC conversion time and data load time for on-card RAM. The BLC-8737 is always in operation, loading RAM with latest data for each channel and updating RAM on each succeeding scan. The data is read with a memory-read instruction (LHLD). Input data appears as 12 bits, right justified in a 16-bit data format. Bipolar data includes extended sign.

If channel data must be known to be more current than 2 milliseconds, the random access feature may be employed. To use this feature it is only necessary to re-write the gain instruction for the desired channel. A gain-set instruction will reset the channel address counter to the addressed channel, and will initiate a data acquisition/conversion cycle. At completion of conversion, an interrupt will signal when current data may be read as outlined above. The interrupt may be set to any, or none, of the eight bus interrupt lines.

The selected analog input is applied to the A/D converter through a software controlled programmable-gain amplifier which provides gains of 1,2,5, or 10, and a sample-and-hold amplifier. A set of movable jumpers allow additional gain multiples of 1, 4 or 10 applied to the above gains. With the ADC jumper selected for +10.24 or ±10.24 full-scale input voltage, the variable gain amplifier permits sampling of analog input voltages as shown in Table I.

Table I. Programmable-Gain Full-Scale Values

Gain Selected		Unipolar	Bipolar Selection
Software	Jumper		
1	1	+10.24	±10.24
2		+ 5.12	+ 5.12
5		+ 2.048	+ 2.048
10		+ 1.024	+ 1.024
1	4	+ 2.56	± 2.56
2		+ 1.28	± 1.28
5		+ 0.512	± 0.512
10		+ 0.256	± 0.256
1	10	+ 1.024	± 1.024
2		+ 0.512	± 0.512
5		+ 0.2048	± 0.2048
10		+ 0.1024	± 0.1024

The only analog input control parameter is the gain setting for each channel. After system initialization, gain must be set for every channel. Part of a post-initialization or system start-up program will be a series of gain-set memory-write instructions, one to each channel address. A two-bit gain word may be written into either byte of the addresses assigned to the input channels. The gain select words are described in Table II.

Table II Gain-Set Data Word

Gain	Data Word								
1	(MSB)	X	X	X	X	X	X	1	1
2		X	X	X	X	X	X	1	0
5		X	X	X	X	X	X	0	1
10		X	X	X	X	X	X	0	0

Analog Output

Two independent analog outputs may be unipolar or bipolar, and provide outputs via 12-bit DACs, according to jumper selections as follows:

0 to +5V
0 to +10V
±2.5V
±5V
±10V
4 to 20mA (source)

The current mode is operational for loop supplies of +12 to +40V. Both output channels are set to minimum scale at system initialization.

Output data is 12-bits, right justified in a 16-bit data field. The address space occupied by the output channels is in the same 2K byte area selected for input channels. Address lines ADR4/ to ADR9/ may be jumper selected anywhere in the 2K byte sector except at those addresses occupied by the input channels. The remaining address bits select the output channel and byte as shown in Table III.

Table III. Output Channel Addressing

Base + Address Bit 3/	2/	1/	0/	Channel
X	X	0	0	Ch1, Low Byte
X	X	0	1	Ch1, High Byte
X	X	1	0	Ch2, Low Byte
X	X	1	1	Ch2, High Byte

DC to DC Converter

The board contains a DC/DC converter to convert the +5V logic supply to the ±15V required by analog ciruitry.

Diagnostic Test

A diagnostic test program is included with BLC-8737 to allow testing and calibration of the analog circuits. Calibration is recommended when a full-scale range jumper is reset (input or output).

Channel Expansion

Sockets are provided to double the number of channels by inserting two multiplexers (LF 13508).

Specifications

Analog Input

Data Channels — 16 single-ended or 8 differential
Expandable to — 32 single-ended or 16 differential
Scan Mode — Sequential
Throughput Rate — 8500 conversions/second
Maximum Data Bandwidth — 200 Hz/ch (16 installed channels)
Full-scale Range —

0–10.24V		±10.24		0–20ma
0–5.12V	0–0.512V	±5.12	±0.512V	with user
0–2.56V	0–0.256V	±2.56V	±0.256V	installed
0–2.048V	0–0.2048V	±2.048V	±0.2048	250 ohm
0–1.024V	0–0.1024V	±1.024V	±0.1024V	resistors

Common Mode Voltage — +10.24V (signal plus common mode)
Overvoltage Protection — 125VAC
Programmable Gain
Software 1, 2, 5, 10
Jumper 1, 4, 10
Input Leakage Current — ⩽ 10nA @ 25°C (16 installed channels)
⩽ 60nA @ 0–55°C (16 installed channels)
Input Resistance — 3K ohms (power OFF)
⩾ 100M ohms (power ON)
Input Capacitance — ⩽ 100pF for ON channel (16 installed channels)
⩽ 10pF for OFF channel
Sample & Hold Feedthrough — ⩽ −80dB @ 200Hz
Crosstalk OFF to ON channel — ⩽ −80dB @ 200 Hz
Common-Mode Rejection ⩾ 60dB @ 200Hz (any gain)
ADC Resolution — 12 bits
Quantizing Error — ±½ LSB
Linearity Error — ⩽ ±½ LSB @ 55°V
⩽ ±1 LSB 0–55°C
Overall Accuracy — ⩽ ±0.05% FSR ± ½ LSB @25°C (Gain = 1)
⩽ ±0.07% FSR ± ½ LSB @25°C (Gain = 2, 5, 10)
Includes 3 sigma noise, linearity, offset and scale errors
No Missing Codes — 0–55°C

Analog Output

Data Channels — 2
Full-Scale Range — 0–5V and 0–10V @ 5mA
±2.5V, ±5V,
and ±10V @ ±5mA
4–20mA sourced (load may be grounded)
Current-Mode Supply Voltage — 12–40V (positive)
Max. Current-Mode Load Resistance (+24V supply) — 800 ohms
DAC Resolution — 12 bits
Linearity Error — (Voltage Mode) ⩽ ±½ LSB @ 25°C
⩽ ±1LSB 0–55°C

Settling Time —	
Voltage Mode	⩽ 4μs to ±0.05% of FSR
Current Mode	⩽ 1ms to 0.05%
Monotonic	0–55°C

Interface

System Bus Interface —	Data, address and control bus signals are TRI-STATE™ or open-collector TTL compatible. Fully BLC/SBC compatible.

Interface

System Bus Interface —	Data, address and control bus signals are TRI-STATE™ or open-collector TTL compatible. Fully BLC/SBC compatible.
Connectors	
System Bus —	86-contact double-sided card-cage edge connector on 0.156" centers.
Analog —	One 50-contact double-sided card-edge connector on 0.1 inch centers for input channels 1–16.
	One 50-contact double-sided card-edge connector on 0.1 inch centers for input channels 17–32.
	One 26-contact double-sided card-edge connector on 0.1 inch centers for output channels.
Recommended Mating Connector (Analog)	50 contact double sided connector on 0.1 inch centers 3M 3415-001 AMP 2-86792-3 26 contact double-sided connector on 0.1 inch centers 3M 3462-0001 AMP 1-583715-1

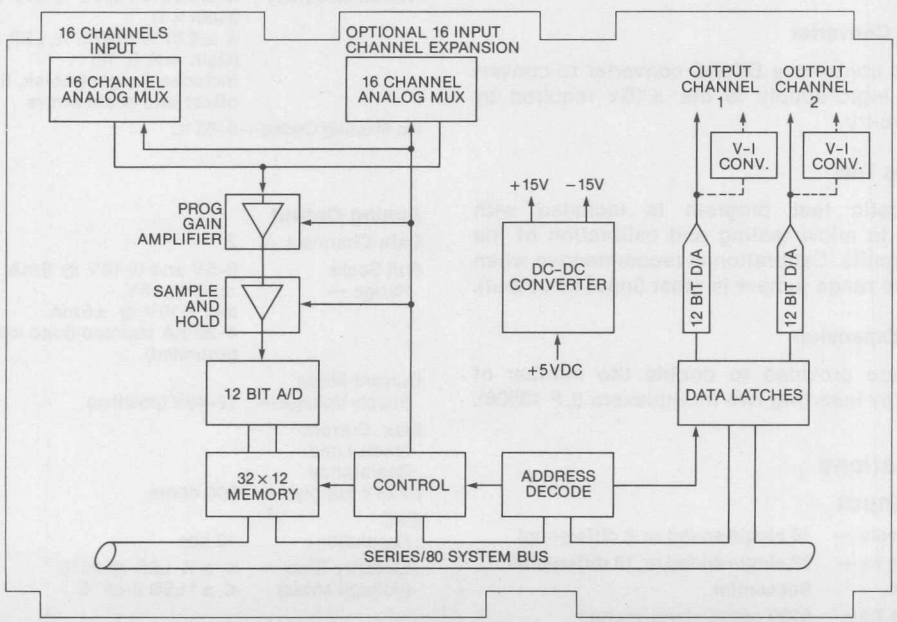
Temperature	0–55°C
Humidity	0–90% non-condensing
Physical —	
Height	6.75" (11.15 cm)
Width	12.00" (30.48 cm)
Depth	0.50" (1.27 cm)
Weight	18 oz. (510.3 g)

Order Information

BLC-8737-1 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, manual, and diagnostic test program in paper tape media.
BLC-8737-3 Analog I/O Board with Memory	Includes 16 single-ended or 8 differential analog input channels, 2 analog voltage or current output channels, manual, and diagnostic test program in paper tape media.

Documentation

420305890-001	BLC-8737 Analog I/O Board with Memory Hardware Reference Manual

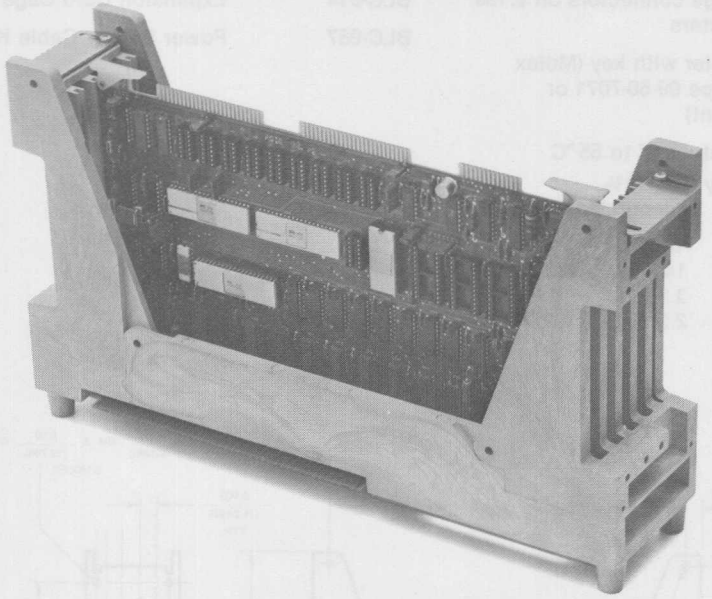


BLC-8737 DIAGRAM

Section 9
Card Cages & Power Supplies

National Semiconductor

BLC-604 and BLC-614 Card Cages



- **Series/80 System Flexibility**
  - 4 board incremental expansion capability
  - Requires only 3.5 inches of vertical space
- **Easy to Use — Includes:**
  - Backplane
  - Power supply connector
  - Threaded mounting holes

Product Overview

The BLC-604 and BLC-614 System Card Cages are ready-made, low-cost chassis for the housing and interconnection of National Semiconductor's Series/80 Board Level Computer products. Both the BLC-604 and BLC-614 Card Cages hold up to four Series/80 boards. The BLC-604 may be used in a stand alone configuration, while the BLC-614 is used as an addition to the BLC-604 when more space is required.

Functional Description

The BLC-604 is a 4-slot molded chassis including a backplane, with data, address and control signal bus, terminating networks, power supply connectors, and a bus extension circuit card edge connector. When more than one card cage is necessary a four slot BLC-614 expansion card cage is plugged into the bus expansion connector on the BLC-604. The BLC-614 contains an expansion connector for cascading additional BLC-614 card cages. The number of card cages to be cascaded is limited only by the bus drive capability or space limitations of the system. A BLC-604 or BLC-614 occupies only 3.5 vertical inches permitting highly compact packaging. The card cages can be conveniently mounted in any one of three planes.

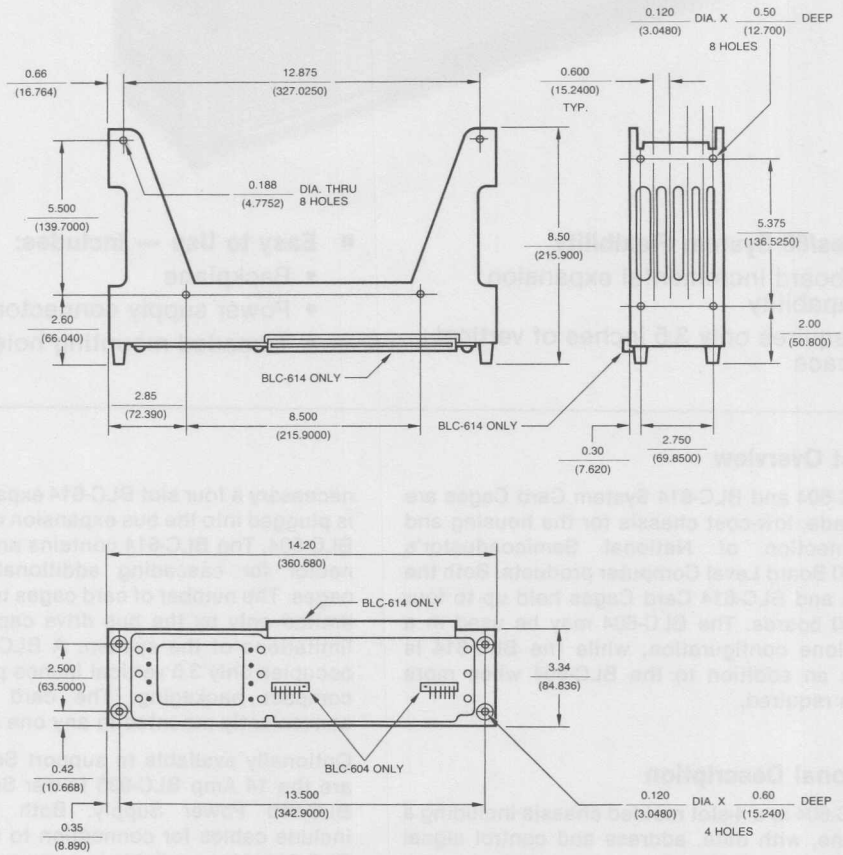
Optionally available to support Series/80 systems are the 14 Amp BLC-635 Power Supply or 30 Amp BLC-665 Power Supply. Both power supplies include cables for connection to the BLC-604 and BLC-614. Also available is a power supply cable kit, the BLC-957, containing 2-foot cables for custom power supply connection to the card cage.

	cage edge connectors on 0.156 inch centers
Power	7-pin wafer with key (Molex crimp type 09-50-7071 or equivalent)

Environmental — Temperature 0° to 55°C
Humidity 0 to 90% non-condensing

Physical —			
	Height	8.5 in.	(21.59 cm)
	Width	14.2 in.	(36.07 cm)
	Depth	3.34 in.	(8.48 cm)
	Weight	2.2 lbs.	(997.92 g)

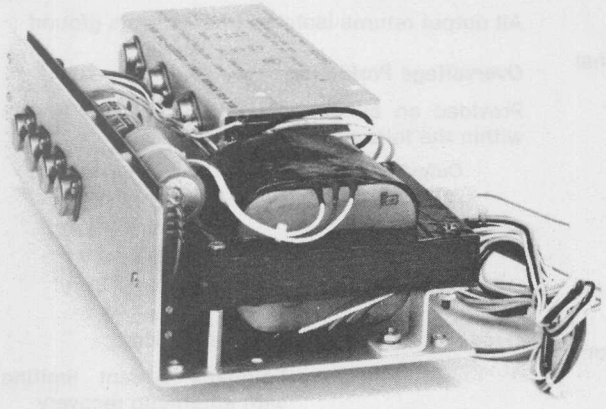
BLC-614	Expansion Card Cage Assembly
BLC-957	Power Supply Cable Kit



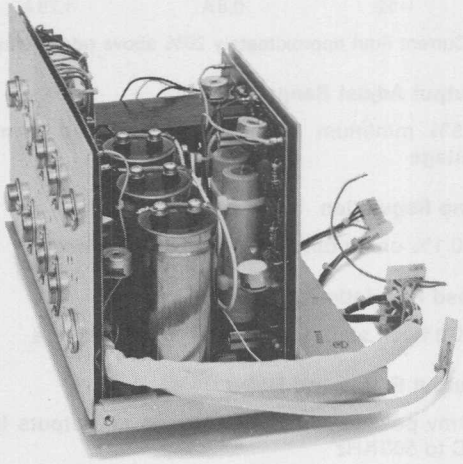
BLC-604 and BLC-614 Diagram

National Semiconductor

BLC-635 and BLC-665 Series/80 Power Supplies



BLC-635



BLC-665

- **Complete Power Supply Systems**
  - ±5, ±12 volt outputs
  - 110-115, 220-230 VAC input power
  - 47-63 Hz input frequency
- **High System Reliability**
  - AC low voltage sensing with TTL level output signal
  - Current limited outputs
  - Output overvoltage protection
- **Compatible with BLC/SBC Series/80 Systems**
  - BLC-635 supplies BLC/SBC CPU and three expansion boards
  - BLC-665 supplies BLC/SBC CPU and seven expansion boards
  - Mating cables for BLC/SBC-604 and 614 System Card Cages
  - BLC-635 — plug-replacement for SBC-635

Product Overview

The BLC-635 and BLC-665 are ready-made, low-cost power supplies for National Semiconductor's Series/80 Board Level Computers. These power supplies provide ±5 and ±12 volts of regulated DC power at maximum current over a temperature range of 0° to +55°C.

The BLC-635 provides power for a fully loaded BLC/SBC CPU with enough additional capacity to supply most configurations of three BLC/SBC memory, I/O, or other expansion boards.

The BLC-665 supplies approximately twice the rated power of the BLC-635. The BLC-665 will power a fully loaded BLC/SBC CPU board and most combinations of seven additional expansion boards.

All outputs are current limited and have overvoltage protection. The AC input is fused for either 100-115 VAC or 200-230 VAC operation.

DC power is carried on cables keyed for compatibility to the BLC-604 System Card Cage. The BLC-635 and BLC-665 utilize circuitry to sense an AC power failure or low line conditions and will generate a TTL compatible signal for orderly system shutdown.

Functional Description

Output Current Rating

VDC	BLC-635	BLC-665
+5	14 A	30 A
−5	0.9 A	1.75 A
+12	2.0 A	4.5 A
−12	0.8 A	1.75 A

Current limit approximately 20% above rated values.

Output Adjust Range

±5% minimum on all outputs around nominal voltage

Line Regulation

±0.1% on all outputs for 10% line change

Load Regulation

±0.1% on all outputs for 50% load change

Output Ripple and Noise

10 mv peak-to-peak maximum on all outputs from DC to 500 KHz

Stability

±0.05% on all outputs for 8 hours at constant line, load, and temperature after 30 minutes of warm-up

Transient Response

±5% on all outputs maximum for less than 50 microseconds with 50% load change

Remote Sensing

Provided at P8 connector for +5 volts

Chassis Ground Insulation

All output returns isolated from chassis ground

Overvoltage Protection

Provided on all outputs and factory set to trip within the following ranges:

Output Voltage	OVP Trip Range
+5V	5.8V to 6.6V
−5V	−5.8V to −6.6V
+12V	14V to 16V
−12V	−14V to −16V

Overload and Short Circuit Protection

+5V — Foldback current limiting with automatic recovery

−5V, +12V, −12V — Current limited to extent no damage will occur for extended overload condition

Specifications

Input Power — 100, 115, 215, 230 VAC ± 10%
47-63 Hz

Input Fusing — 100/115 VAC 3.0 A slow blow
200/230 VAC 1.5 A slow blow

Connectors —

	BLC-635/665 Connectors			Recommended Mating Parts		
		Part Number			Part Number	
	Type	Molex	Amp	Type	Molex	Amp
AC Input (P2)	Connector Pin	03-09-2052 02-09-2118	N/A	Connector Pin	08-09-1052 02-09-1118	N/A
DC Output (P6, P8)	Connector Pin Polarizing Key	09-50-7071 08-50-0106 15-04-0219	87159-7 87023-1 87116-2	Right Angle Connector Assembly	09-66-1071	87194-6
"AC Low" Detection (J3)	Connector Assembly	09-67-1072 or 09-66-1071	87262-7	Connector Pin Polarizing Key	09-50-7071 08-50-0106 15-04-0219	87159-7 87023-1 87116-2

Environmental — Temperature 0° to 55 °C
Humidity 0 to 90%
non-condensing

Physical —

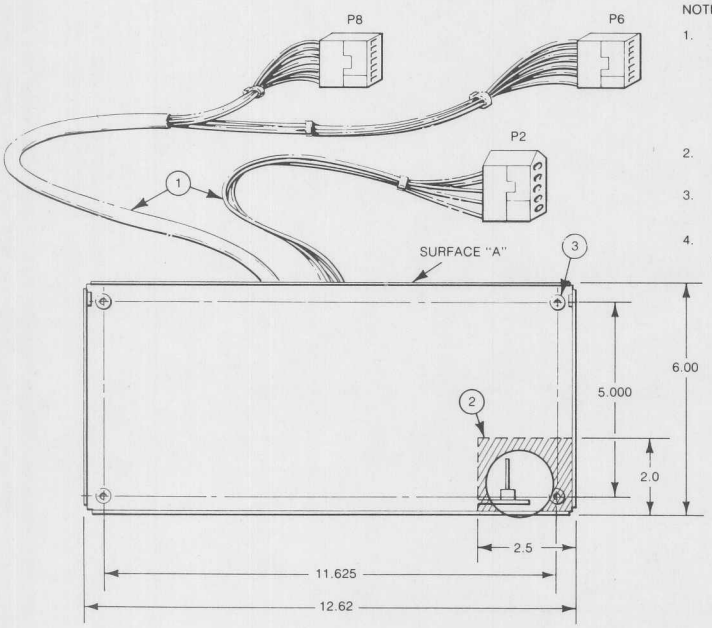
	BLC-635	BLC-665
Height	3.19 in. (8.1 cm)	6.62 in. (16.8 cm)
Width	6.03 in. (15.3 cm)	6.50 in. (16.5 cm)
Depth	12.65 in. (32.1 cm)	12.65 in. (32.1 cm)
Weight	13 lb. (5.9 kg)	21 lb. (9.6 kg)

Order Information

BLC-635	14 A Power Supply, includes cables for connection to card cage.
BLC-665	30 A Power Supply, includes cables for connection to card cage.

Documentation

420305489-001	BLC-635 Power Supply User's Manual
420305220-001	BLC-665 Power Supply User's Manual



NOTES:

1. Harness lengths are from center of surface "A" to connector
   a. DC OUTPUT 24 inches to P6 conn.
   b. DC OUTPUT 16 inches to P8 conn.
   c. AC INPUT 12 inches to P2 conn.
2. Location of "AC LOW" signal connector is within cross hatched volume, orientation may vary.
3. All four mounting holes threaded for 8-32 machine screws.
4. BLC-665 has 2 each connectors P6, P8 to enable connection to two card cages.

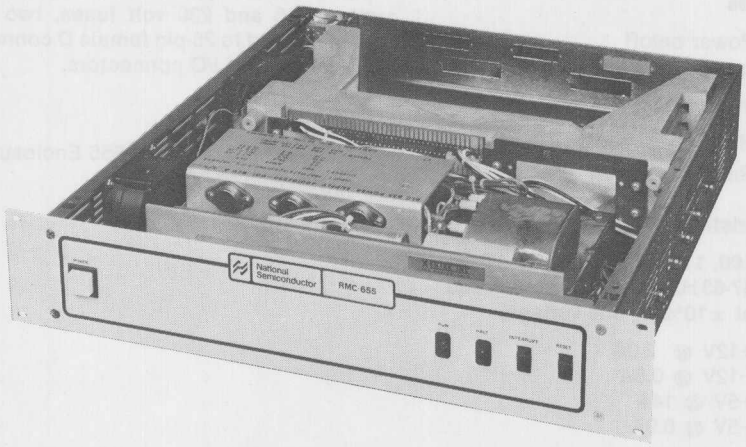
BLC-635 Diagram

Section 10
Rack Mountable Microcomputer Systems

Section 10
Rack Mountable Microcomputer Systems

National Semiconductor

RMC-655
System Chassis



- **Self-Contained Rack Mountable Package for OEM Applications**
  - BLC-635 Power Supply
  - BLC-604 4-Slot Card Cage
- **Front Panel with Power, Reset, and Interrupt Switches, and Halt and Run Status Indicators**
- **Rear Panel with Provision for User Installed Connectors**
- **Compatible with Standard BLC/SBC Series/80 Products**
- **Replacement for Intel's SBC 655 System Chassis**

Product Overview

The RMC-655 provides an economical, off-the-shelf housing for computer systems. The RMC-655 can support any MULTIBUS™ compatible product. It comes equipped with ±5 and ±12 volt power supply, DC over-voltage protection, and AC low-line detection circuitry. Two fans provide cooling within the RMC-655. The front panel features interrupt and reset switches, and halt and run indicators.

Functional Description

The BLC-635 Power Supply provides regulated DC outputs of ±5 and ±12 volts. All outputs feature current limiting and over-voltage protection. Logic provided in the power supply will sense an AC power failure or low-line condition and generate a TTL compatible signal for an orderly system shutdown sequence. The power supply is connected to the 4-slot card cage by a mating cable set.

The power on/off and reset switches on the front panel allow external control of the computer system. Ample room is provided for the addition of user unique controls in addition to those provided.

The RMC-655 is ideal for applications requiring up to four Multibus boards.

*MULTIBUS™ is a trademark of Intel Corporation.

Width	19 in.	(48.26 cm)
Depth	20 in.	(50.8 cm)
Weight	37 lb.	(16.8 kg)

Front Panel Features

Switches — Power on/off
Reset
Interrupt

Indicators — Halt
Run

Electrical Characteristics

AC input — 100, 115, 215, 230 volts AC @ 47-63 Hz (over-voltage invoked at ±10% of line voltage)

DC output — +12V @ 2.0A
−12V @ 0.8A
+5V @ 14A
−5V @ 0.9A

Environmental Characteristics

Temperature — 0°C to 55°C

Humidity — 0 to 90%, non condensing

RMC-655E	System Chassis, 200-230 VAC, 50 Hz

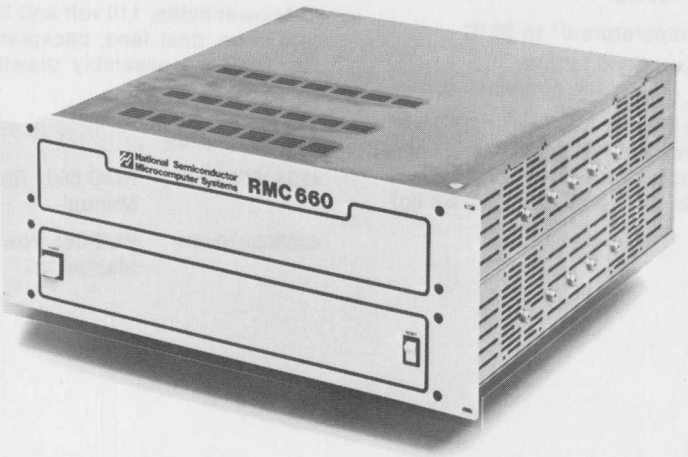
Both systems include 4-slot card cage and backplane assembly, BLC-635 Power Supply, power cord, 115 and 230 volt fuses, two fans, RS232C cable (board to 25-pin female D connector), and two 50-pin parallel I/O connectors.

Documentation

420306257-001	RMC-655 Enclosure User's Manual

National Semiconductor

RMC-660
System Chassis



- **Allows Large OEM Configuration of Series/80 Products**
  - 8-slot card cage
  - Heavy duty 30 Amp power supply
- **Front Panel with Power and Reset Switches for Control**
- **Rear Panel Accepts a Variety of User Connectors**
- **Plug-replacement for SBC-660 System Chassis**

Product Overview

The RMC-660 System Chassis supports Series/80 Board Level Computers and the full complement of expansion boards. The chassis occupies 7 inches of vertical rack space in a standard 19-inch RETMA rack. The System Chassis includes a BLC-665 Heavy Duty Power Supply, cooling fans, and an 8-slot card cage including a printed circuit board bus.

Functional Description

The BLC-665 Heavy Duty Power Supply provides regulated DC outputs of ±5 and ±12 volts. Current limiting and overvoltage protection is provided on all outputs. Logic provided in the power supply senses an AC power failure or low line condition and generates a TTL compatible signal for an orderly system shutdown sequence. The power supply is connected to the 8-slot card cage by a mating cable set.

The front panel contains a power on-off switch and a reset switch which connects to the system bus of a CPU for external system control.

The RMC-660 is ideal for OEM applications requiring up to 8 boards.

Specifications

Refer to detailed specifications for BLC-665 Heavy Duty Power Supply.

Front Panel Switches —	Power On/Off Reset		
Input Power —	100, 115, 215, 230 VAC ± 10% 47-63 Hz		
Environmental —	Temperature 0° to 55°C Humidity 0 to 90% non-condensing		
Physical —	Height	7.00 in.	(17.8 cm)
	Width	19.00 in.	(48.3 cm)
	Depth	20.00 in.	(50.8 cm)
	Weight	49 lb.	(22.2 kg)

Order Information

RMC-660	System Chassis, 110-115 VAC, 60 Hz.
RMC-660E	System Chassis, 200-230 VAC, 50 Hz.

Both systems include: card cage and backplane assembly, BLC-665 Heavy Duty Power Supply, 115 volt power cable, 115 volt and 230 volt fuses, 8-slot card cage, dual fans, backplane schematic drawing, RMC-660 assembly drawings and documentation.

Documentation

420305561-001	RMC-660 Enclosure User's Manual
420302220-001	BLC-665 Power Supply User's Manual